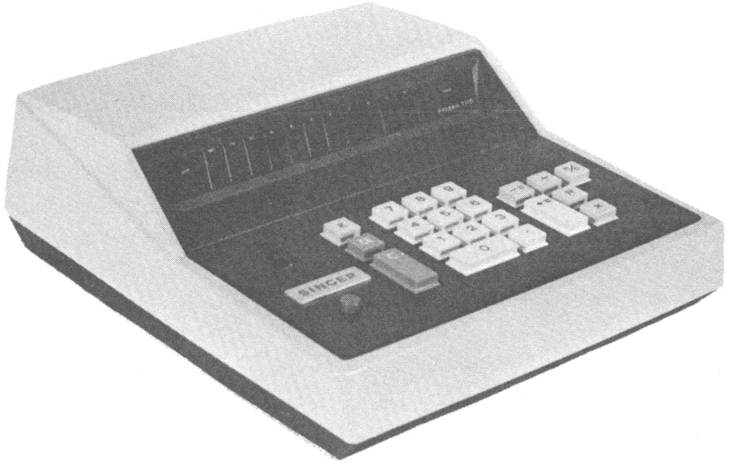
1115 ELECTRONIC CALCULATOR

SERVICE
MANUAL



SINGER
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TPD-169SL

PREFACE

The intent of this manual is to provide maintenance information to trained field personnel. When used for training purposes, this manual must be supplemented with a course curriculum. The manual itself is not designed for self instruction.

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SECTION 1

GENERAL DESCRIPTION

SECTION CONTENTS

1115 ELECTRONIC CALCULATOR

GENERAL DESCRIPTION

A. APPEARANCE

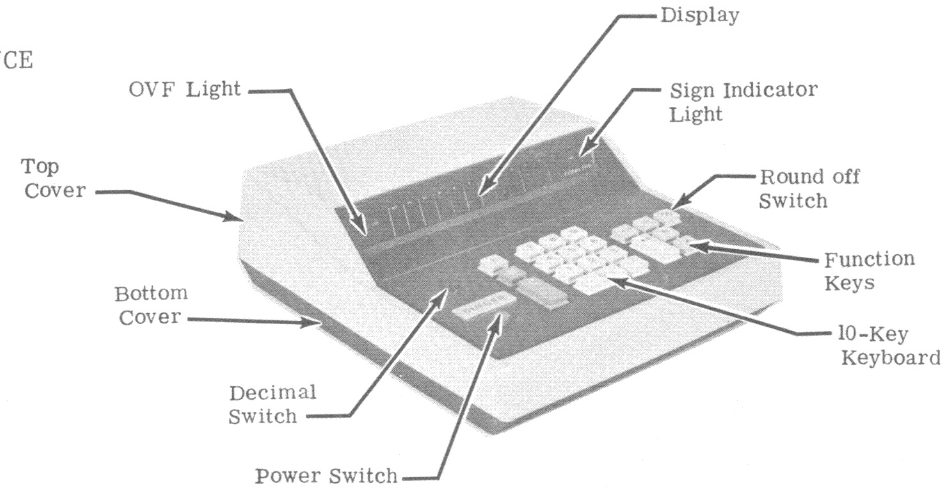


FIGURE 1-1

The 1115 Electronic Calculator (Figure 1-1) is a small, light weight, high speed portable desk calculator featuring: a 12-digit Nixie type, number indicating tube display, 10-key keyboard, and integrated (IC) electronic circuitry for long life and maximum reliability.

B. SPECIFICATIONS

Size:	10" wide, 13" deep, and 4" high (approx).
Weight:	10 lbs.
Keyboard:	10-key type. Any number can be entered (maximum of 12 digits) using the ten digit keys (0-9) and the Decimal Point key if applicable. The Function keys are arranged around the Digit keys in a manner that provides maximum operator facility and ease of operation.
Decimal System:	Floating Input/Fixed Output (Decimal Switch Positions: 0, 2, 5)
Speed:	The longest arithmetic problem in:

Addition and Subtraction	0.05 sec.
Multiplication	0.4 sec.
Division	0.4 sec.

Reliability:	Use of the latest state of the art integrated circuit chips, transistors, and diodes insures maximum reliability and serviceability.
Power Source:	The 1115 can be connected to any standard, grounded 115 VAC outlet. Transformer taps are provided for 100V, 110V, 117V, & 120V (50/60 Hz) operation. Optional voltages are available on special order.
Power Consumption:	12 watts
Ambient Temperature:	0-40° C (32-104° F)

C. KEY FUNCTIONS

The Keyboard keys (Figure 1-2) can be grouped by function as: Digit, Arithmetic, and Data Handling. The Digit keys are used in entering numbers; the Arithmetic keys are used in operations which involve computations; and the Data Handling keys shift numbers between registers, or clear numbers from the machine.

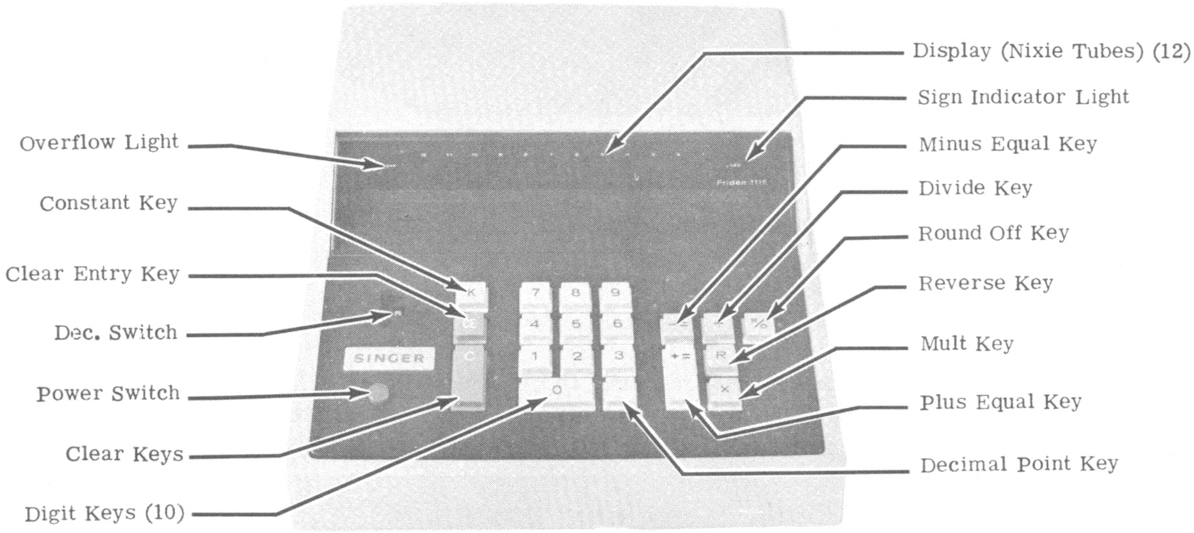


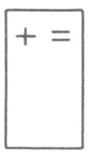
FIGURE 1-2

1. DIGIT KEYS

Numbers are entered into the 1115 data loop digit-by-digit by use of the digit keys. Since numbers can contain decimal digits, the decimal point key is also considered to be in the digit group because it is used for a decimal number entry.

2. ARITHMETIC KEYS

The arithmetic keys enable and initiate the arithmetic operations that will be performed with and on the numbers. Briefly their functions are:



a. PLUS EQUAL KEY. Depression of this key initiates the addition, multiplication, and division functions. In an Add function the contents of R2 are added to R3. In Mult or Divide, the answer is produced in R2 as a result of repeat addition or repeat subtraction.

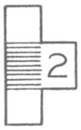
When the machine is not conditioned to multiply or divide, depression of this key causes R2 to be added to R3 with the result in R2 and the 2nd Entry to be retained in R3. (Note: In the 1115, the 2nd Entry will always be retained in R3 following an Add, Subtract, Mult, or Divide.) If the machine is conditioned to multiply and no data has been entered into R2 since the multiply conditioning, depression of this key causes: R2 to transfer to R3 with R2 being unchanged; R3 to be multiplied by R2; the final product in R2 and the entered number retained in R3.

If the machine is conditioned to multiply and data has entered R2 since the multiply conditioning, R3 is multiplied by R2 with the product in R2 and the 2nd Entry retained in R3. If the machine is conditioned to divide, depression of this key causes R2 to be divided by R3 with the quotient in R2 and the 2nd Entry retained in R3.

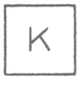
b. MINUS EQUAL KEY. Depression of this key initiates the subtraction, multiplication, and division functions. When the machine is not conditioned to multiply or divide, depression of this key causes R3 to be subtracted from R2 with the result in R2 and the 2nd Entry in R3. If the machine is conditioned to multiply, multiplication occurs as defined for Plus Equal, except prior to multiplication, the sign of R2 is changed. If the machine is conditioned to divide, division will occur as defined for the Plus Equal key except prior to division, the sign of R2 is changed.

c. MULT KEY. Depression of this key terminates the digit entry and conditions the machine to multiply. However, when the machine is already conditioned to multiply, or divide, by a prior Mult or Divide key depression, and the Mult key is again depressed following a digit entry, the machine will perform the function corresponding to its prior conditioning. This will also establish a Mult condition for the next machine operation.

d. DIVIDE KEY. Depression of this key terminates the digit entry and conditions the machine to divide. However, when the machine is already conditioned to multiply, or divide, by a prior Mult or Divide key depression, and the Divide key is again depressed following a digit entry, the machine will perform the function corresponding to its prior conditioning. This will also establish a Divide condition for the next machine operation.



e. DECIMAL SET SWITCH. This is a slide type switch having three positions for setting the decimal point at 0, 2, or 5. Decimal control of the final answer is defined by the setting of the Decimal Set Switch.



f. CONSTANT KEY (K). This is a latch down type key used for retaining a constant multiplier or a constant divisor. It also retains the command to multiply or divide until a Mult or Divide key is depressed to change the constant function. Briefly, the Constant key is used as follows:

A x B =	A ÷ B =	B^2
C x B =	C ÷ B =	B^3
D x B =	D ÷ B =	B^4

When the "K" key is in the latched position (down), the first step of each key function is normal as: A [X] B [+=] ; A [÷] B [+=] ; B [X] [+=] . After the first mult or divide key function is completed, the key function in use is automatically retained and the "B" factor becomes a constant. Under this condition, entry of a new number (C or D) factor causes the contents of the previous product in R2 to be cleared and the new entry (C or D) goes into R2 while the constant factor "B" is retained in R3. Depression of the [+=] key causes the second calculation to be performed. In other words, when the "K" key is latched down, depressing the [+=] key or the [-=] key always causes R3 to be multiplied by R2 (for the multiplication condition); or R2 to be divided by R3 (for the divide condition). The operation will continue in this manner until another Mult or Divide key is depressed. Then, the constant condition set up by the "K" key is cleared and normal machine operation is established even though the "K" key remains latched down.

[R/O]

g. ROUND OFF SWITCH. The Round Off Switch is a latch down type switch which enables a decimal round off of the LSD of the answer in R2 if necessary. When the R/O switch is latched down and the decimal number to the right of the LSD in R2 is greater than "4", a "1" is added to the LSD in R2.

3. DATA HANDLING KEYS

Using the data handling keys results in the shifting of numbers between registers; and the clearing of numbers from R2 and R3. The function of the Data Handling keys is explained briefly as follows:

[R]

a. REVERSE KEY. Depression of this key exchanges the contents of R2 and R3. The algebraic sign of a register is considered as part of its contents.

[C]

b. CLEAR KEY. Depression of this key causes R1, R2, and R3 to be cleared, and all control flip-flops will reset. If the machine is in an overflow condition, the overflow light will be turned off and the keyboard will be unlocked electrically.

[CE]

c. CLEAR ENTRY KEY. Depression of this key causes R2 and R1 to be cleared. If the machine is in an overflow condition, the overflow light will be turned off and the keyboard will be unlocked electrically.

4. POWER SWITCH

A push-on, push-off type switch located in the lower left corner of the keyboard is used to turn the power on and off. Turning the machine power on automatically causes all registers to be cleared to zero, the sign of all registers to be positive, and the decimal position of all registers to be transferred to the right of the lowest displayed ordinal position.

5. INDICATING LIGHTS

a. OVERFLOW LIGHT. The Overflow light located at the left side of the display panel comes on:

(1) When data entry to R2 exceeds 12 digits or 11 decimal digits.
(2) When the integer portion of the answer developed in R2 minus the number of decimal places defined by the Decimal Switch exceeds 12 digits.

When the overflow condition is indicated, the keyboard is immediately interlocked electrically. The overflow condition is cleared by the Clear key or the Clear Entry key.

b. NEGATIVE LIGHT. The Negative Light located at the right side of the display panel comes on:

(1) When the data is entered in R2 by the Minus Equal key.
(2) When the output (answer) is negative (as governed by the rules of algebraic signs).

SECTION 2

CALCULATING METHODS

SECTION CONTENTS

1115 ELECTRONIC CALCULATOR

CALCULATING METHODS

A. GENERAL

This section of the manual describes the various calculations possible with the 1115 Electronic Calculator. Sample problems are provided to illustrate the process and to give the CSRep a working knowledge of the machine operation which is essential to understanding the machine logic and an aid in troubleshooting.

Listed below are several pertinent points that should be noted.

(1) The machine has a floating decimal point input and a fixed point output system.

(2) When an answer or ar entry is negative, it is indicated with a minus sign.

(3) The number recalled by the Reverse key is used the same as a digit entry.

(4) Repeated depression of the Mult and Divide keys merely changes the order of the operation to coincide with the last depressed key,

B. ADDITION

Addition is accurate up to 12 digits. Depressing the Clear key is necessary before each calculation.

PROBLEMS:

(1) Addition without decimals under decimal preset position of 2.

946 + 583 + 123 = 1652.00

SOLUTION	INDEX IN KEYBOARD	TOUCH FUNCTION KEYS IN SEQUENCE	DISPLAY
1) 946+583+123=1652		2 R/O ↓ C	
	946	+=	946.00
	583	+=	1529.00
	123	+=	1652.00

B. ADDITION (Cont.)

(2) Addition with decimal under decimal preset position of 2.

2.63 + 0.574 + 0.02 = 3.22

SOLUTION	INDEX IN KEYBOARD	TOUCH FUNCTION KEYS IN SEQUENCE	DISPLAY
2) 2.63+0.57+0.02=3.22		2 R/O ↓ C	
	2.63	+=	2.63
	0.57	+=	3.20
	0.02	+=	3.22

C. SUBTRACTION

Subtraction is accurate up to 12 digits. Depressing the Clear key is necessary before each calculation.

PROBLEMS:

(1) Subtraction without decimals under decimal preset position of 2.

657 - 492 = 165.00

SOLUTION	INDEX IN KEYBOARD	TOUCH FUNCTION KEYS IN SEQUENCE	DISPLAY
1) 657 - 492 = 165		2 R/O ↓ C	
	657	+=	657.00
	492	-=	165.00

C. SUBTRACTION (Cont.)

(2) Subtraction and Addition under decimal preset position of 2.

-530 + 829 = 299.00

(3) Subtraction with True Credit Balance under decimal preset position of 2.

139 - 567 = -428.00

SOLUTION	INDEX IN KEYBOARD	TOUCH FUNCTION KEYS IN SEQUENCE	DISPLAY
2) -530 + 829 = 299		2 (decimal switch) R/O ↓ C	
	530	-=	530.00-
	829	+=	299.00
3) 139 - 567 = -428		2 (decimal switch) R/O ↓ C	
	139	+=	139.00
	567	-=	428.00-

D. MULTIPLICATION

Multiplication is accurate up to 12 digits and depressing the Clear key is not necessary before each calculation. In chain multiplication (and regular multiplication) if the integer portion of the result developed by multiplying the previous product and the next multiplier exceeds 12 digits (minus the decimal preset number) it will be necessary to set the decimal set switch to "0".

In Chain Multiplication, successive products can be multiplied with or without using the Plus Equal key each time. For example:

123 x 456 x 789 += .

D. MULTIPLICATION (Cont.)

PROBLEMS:

(1) Multiplication without decimals

12 x 24 = 288

(2) Multiplication with decimals

6.123 x 47.89 = 293.23047

(3) Chain multiplication

3.69 x 65.41 x 1.479 = 356.97572

(4) Multiplication with negatives

-369 x 682 x (-34) = 8556372

SOLUTION	INDEX IN KEYBOARD	TOUCH FUNCTION KEYS IN SEQUENCE	DISPLAY
1) 12x24 = 288		[2] [R/O] ↓	
	12	[X]	12.
	24	[+=]	288.00
2) 6.123x47.89		[2] [R/O] ↓	
	6.123	[X]	6.123
	47.89	[+=]	293.23
3) 3.69x65.41x1.479 = 356.9757291		[2] [R/O] ↓	
	3.69	[X]	3.69
	65.41	[X]	241.36
	1.479	[+=]	356.97
or another way		[2] [R/O] ↓	
3.69x65.41 = 241.36	3.69	[X]	3.69
	65.41	[+=]	241.36
241.36x1.479 = 356.97		[X]	241.36
	1.479	[+=]	356.97
4) -369x682x(-34)=8556372		[2] [R/O] ↓ [C]	
	369	[-=]	369.00
		[X]	369.00
	682	[X]	251658.00
	34	[-=]	8556372.00

E. CONSTANT MULTIPLICATION

The Constant key "K" is used for this calculation. Normal operation, except Add and Subtract, can be accomplished even though the "K" key is latched down. See page 1-3 for an explanation of the "K" key operation.

PROBLEMS:

GROUP 1

(1) 123 x 4.56 = 560.88

(2) 563 x 4.56 = 2567.28

(3) 213 x 4.56 = 971.28

Note: The number "4.56" is the constant multiplier

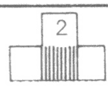
GROUP 2 (Involution)

(1) 25^2 = 625

(2) 25^3 = 15625

(3) 25^4 = 390625

Note: In this case, the constant multiplier is "25".

SOLUTION	INDEX IN KEYBOARD	TOUCH FUNCTION KEYS IN SEQUENCE	DISPLAY
1) 123x4.56=560.88		 R/O ↓ K ↓	
	123	X	123.
	4.56	+=	560.88
563x4.56=2567.28	563	+=	2567.28
213x4.56=971.28	213	+=	971.28
2) 25^2 = 625	25	X	25.
		+=	625.00
25^3 = 15625		+=	15625.00
25^4 = 390625		+=	390625.00

F. DIVISION

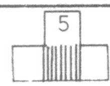
Division is accurate up to 12 digits. Touching the Clear key is not necessary before each calculation. In chain division, successive quotients can be divided without using the Plus Equal key each time.

PROBLEMS:

(1) Division without decimals — 145 ÷ 12 = 12.08333

(2) Division with Decimals — 4962.184 ÷ 13.2 = 375.92303

(3) Chain Division — 369 ÷ 123 ÷ 456 = 0.00658

SOLUTION	INDEX IN KEYBOARD	TOUCH FUNCTION KEYS IN SEQUENCE	DISPLAY
1) 145÷12=12.08333		 R/O ↓	
	145	÷	145.
	12	+=	12.08333
2) 4962.184÷13.2	4962.184	÷	4962.184
=375.923030	13.2	+=	375.92303
3) 369÷123÷456	369	÷	369.
=0.006578	123	÷	3.00000
	456	+=	0.00658
Or another way 369÷123=3	369	÷	369.
	123	+=	3.00000
3÷456=0.006578		÷	3.00000
	456	+=	0.00658

G. CONSTANT DIVISOR

The Constant key "K" is used for this calculation. Normal operation, except Add and Subtract may be accomplished even though the "K" key is latched down. See Page 1-3 for an explanation of the "K" key function.

PROBLEMS:

(1) 297 ÷ 1364 = 0.21774

(2) 6428 ÷ 1364 = 4.71261

(3) 1000 ÷ 1364 = 0.73314

Note: The number "1364" is the constant divisor.

(4) $\frac{12367}{12} = 1030.58333$

(5) $\frac{12367}{12^2} = 85.88194$

(6) $\frac{12367}{12^3} = 7.15683$

Note: The number "12" is the constant divisor.

SOLUTION	INDEX IN KEYBOARD	TOUCH FUNCTION KEYS IN SEQUENCE	DISPLAY
		5 R/O ↓ K ↓	
1) 297÷1364=0.21774	297	÷	297
	1364	+=	.21774
2) 6428÷1364=4.71261	6428	+=	4.71261
3) 1000÷1364=0.73314	1000	+=	.73314
4) $\frac{12367}{12}$ 1030.58333	12367	÷	12367.
	12	+=	1030.58333

G. CONSTANT DIVISOR (Cont.)

SOLUTION	INDEX IN KEYBOARD	TOUCH FUNCTION KEYS IN SEQUENCE	DISPLAY
5) $\frac{12367}{12^2}$ = 85.88194		[+=]	85.88194
6) $\frac{12367}{12^3}$ = 7.15683		[+=]	7.15683

H. ROUND OFF AND TRUNCATE

Round Off and Truncate action is performed on the digit to the right of the digit in the lowest decimal position displayed. The answer will be rounded off or truncated depending on the position of the Round Off Switch. That is, in a Round Off calculation, the Round Off Switch must be preset to the position of R/O prior to starting the calculation. If the Round Off Switch is not preset to the position of R/O, the answer will be truncated instead.

Also, if the decimal digit numbers of the entry are greater than the Decimal Switch setting, the entry number will be rounded off or truncated by depression of the Plus Equal key. The number displayed will be defined by the Decimal Switch setting.

PROBLEMS: (Decimal Switch set at "2")

(1) Addition and Subtraction under round off condition.

5.372 + 17.369 - 1.234 = 21.51

(2) Multiplication and Division under round off and truncate condition.

45.769 x 3.52 = 161.11 } Rounding Off
45.769 ÷ 3.52 = 13.00 }

45.769 x 3.52 = 161.10 Truncate

H. ROUND OFF AND TRUNCATE (Cont.)

SOLUTION	INDEX IN KEYBOARD	TOUCH FUNCTION KEYS IN SEQUENCE	DISPLAY
1) 5.372+17.369-1.234		2 · R/O ↓ · C	
=21.51	5.372	+=	5.37
	17.369	+=	22.74
	1.234	-=	21.51
2) 45.769x3.52=161.11		2 · R/O ↓	
	45.769	X	45.769
	3.52	+=	161.11
3) 45.769x3.52=161.10		R/O ↑	
	45.769	X	45.769
	3.52	+=	161.10
4) 45.769÷3.52=13.00	45.769	÷	
	3.52	+=	13.00

I. COMBINED CALCULATIONS

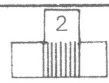
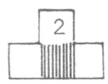
Examples of combined calculations are shown in the three problems that follow.

PROBLEMS:

(1) $123 \times 45.6 \div 78.9 - 1.47 + 25.76 = 95.3774$

(2) $\frac{1000}{(160+320+102)} = 1.7182$

(3) $\frac{(1+0.05)^5 - 1}{0.05} \times 12300 = 67965.264375$

SOLUTION	INDEX IN KEYBOARD	TOUCH FUNCTION KEYS IN SEQUENCE	DISPLAY
1) 123x45.6÷78.9-1.47 +25.76=95.3774		 [R/O] ↓	
	123	[X]	123.
	45.6	[÷]	5608.80
	78.9	[+=]	71.09
	1.47	[-=]	69.62
	25.76	[+=]	95.38
2) $\frac{1000}{(160+320+102)} = 1.7182$		 [R/O] ↓ [C]	
	160	[+=]	160.00
	320	[+=]	480.00
	102	[+=]	582.00
		[÷]	582.00
	1000	[R]	582.00
		[+=]	1.72

I. COMBINED CALCULATIONS (Cont.)

SOLUTION	INDEX IN KEYBOARD	TOUCH FUNCTION KEYS IN SEQUENCE	DISPLAY
3) $\frac{(1+0.05)^{5} - 1}{0.05} \times 12300$		5 R/O ↓ K ↓ C	
= 67965.264375	1	+=	1.00000
	0.05	+=	1.05000
		X	1.05000
		+=	1.10250
		+=	1.15763
		+=	1.21551
		+=	1.27629
		K ↑	1.27629
	1	-=	0.27629
		÷	0.27629
	0.05	X	5.52580
	12300	+=	67967.34000

SECTION 3

LOGIC ELEMENTS

SECTION CONTENTS

A. COMPOSITION OF FUNDAMENTAL CIRCUIT

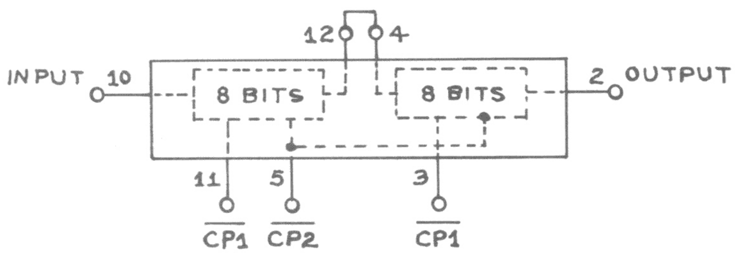
The logic circuits of this machine are composed primarily of eight types of MOS (Metal Oxide Semiconductor) IC (integrated circuit) packaged in dual-in-line circuit chips. Other circuits in the machine are composed of discrete components such as diodes, transistors, etc.

Shown in the Table below are the 8 MOS IC chips used in the machine and their circuit function. A brief explanation of each chip is also included here to familiarize the CSRep with their general function.

Type of IC	Circuit Function
HD 3101	dual 8-bit quasi-static shift register
HD 3103	five MOS FETs (Inverters)
HD 3104	dual 4 input AND gate + two inverters
HD 3106	dual 2 input & a dual 3 input AND gate
HD 3107	quadruple quasi-static D type flip-flop
HD 3109	60 + 4 + 4 bits dynamic shift register (with control gates)
HD 3112	delayed full adder
HD 3115	triple quasi-static RSS flip-flop

1. HD 3101 (Dual 8-bit Shift Register)

A dual 8-bit shift register which is connected in a series configuration to form a 16-bit shift register as shown in Figure 3-1.

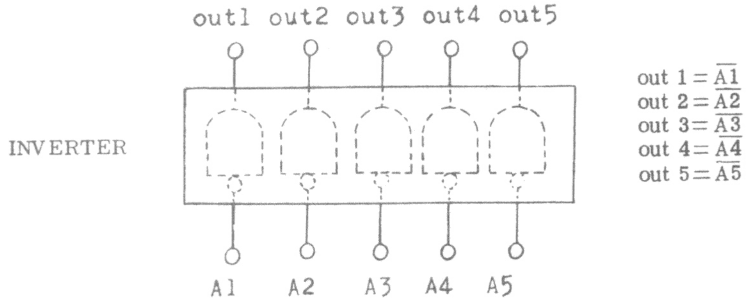


HD 3101

FIGURE 3-1

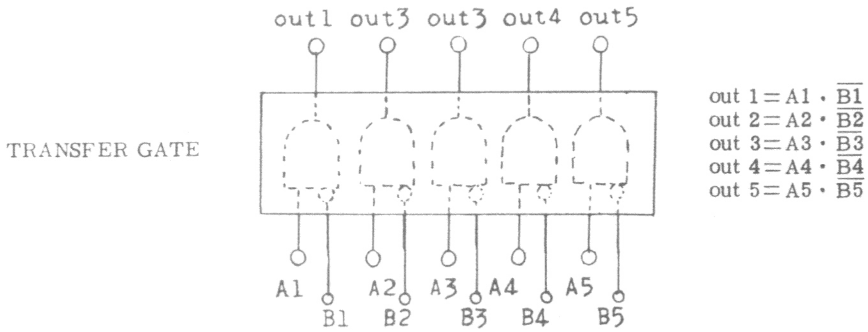
2. HD 3103 (5 MOS FET's)

This IC contains 5 MOS FET's which are used as inverters (Figure 3-2) or as transfer gates (Figure 3-3).



HD 3103

FIGURE 3-2

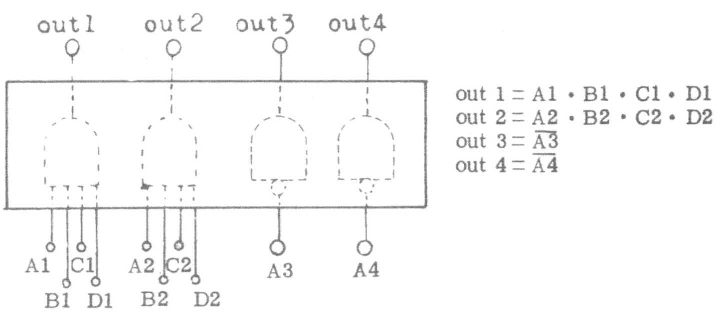


HD 3103

FIGURE 3-3

3. HD 3104 (Dual 4-input AND gate plus 2 Inverters)

This IC is composed of dual 4-input AND/OR gates and 2 Inverters. The gate circuits operate as AND circuits when Logic 1 corresponds to "0" volts and operate as OR gates when Logic 0 correspond to "0" volts (Figure 3-4).

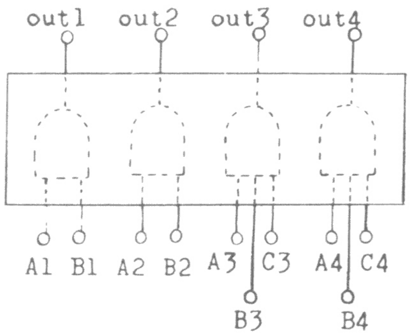


HD 3104

FIGURE 3-4

4. HD 3106 (Dual 3-input AND/OR gate and Dual 2-input AND/OR gate)

This IC is composed of dual 3-input AND/OR gate circuits and dual 2-input AND/OR gates which are used extensively in the various logic circuits of the machine (Figure 3-5).



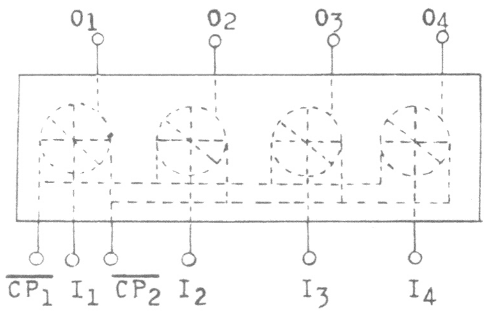
out1=A1·B1
out2=A2·B2
out3=A3·B3·C3
out4=A4·B4·C4

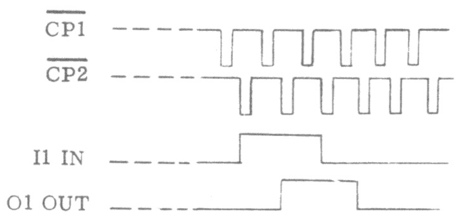
HD 3106

FIGURE 3-5

5. HD 3107 (4 "D" type Flip-Flops)

This IC is composed of 4 "D" type FFs which can be used as individual flip-flops or if connected in series, can be used as a 4-bit shift register (Figure 3-6).





Independent "D" type Flip-Flop Operation

Connections for operation as a 4-bit shift register are as follows:

O_1 to I_2

O_2 to I_3

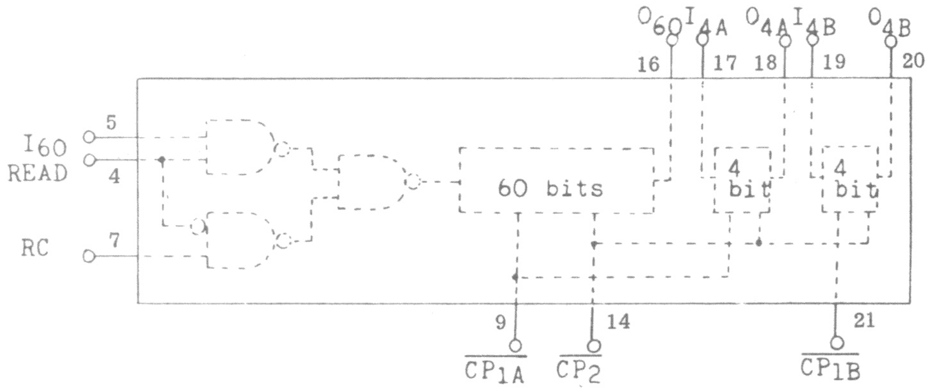
O_3 to I_4

HD 3107

FIGURE 3-6

6. HD 3109 (60 +4 +4-Bit Dynamic Shift Register)

This IC is called a Medium Scale Integrated Circuit (MSI) and contains a 68-bit shift register (60 + 4 + 4). That is, the IC can retain 68 bits of data consisting of 17 4-bit (BCD) digits in a dynamic shift register (Figure 3-7).



HD 3109

FIGURE 3-7

BASIC FAS TRUTH TABLES

ADD

X	Y	C	FA OUT	FC IN
0	0	0	0	0
1	0	0	1	0
0	1	0	1	0
1	1	0	0	1
0	0	1	1	0
1	0	1	0	1
0	1	1	0	1
1	1	1	1	1

SUB

X	Y	C	FA OUT	FC IN
0	0	0	0	0
1	0	0	1	0
0	1	0	1	1
1	1	0	0	0
0	0	1	1	1
1	0	1	0	0
0	1	1	0	1
1	1	1	1	1

X = X input
Y = Y input
C = CONDITION OF CARRY (FC)

FA OUT = SUM ADDER OUTPUT
FC IN = CARRY ENABLE INPUT

FAS COMPENSATION TRUTH TABLES

ADD

XC1	Ff	HC	Xo	$\overline{BT4}$ HC ENABLE
0	0	0	0	0
1	0	0	1	0
0	1	0	1	0
1	1	0	0	1
0	0	1	1	0
1	0	1	0	1
0	1	1	0	1
1	1	1	1	1

SUB

XC1	Ff	HC	Xo	$\overline{BT4}$ HC ENABLE
0	0	0	0	0
1	0	0	1	0
0	1	0	1	1
1	1	0	0	0
0	0	1	1	1
1	0	1	0	0
0	1	1	0	1
1	1	1	1	1

XC1 = LSD OF DIGIT FROM 4-BIT REGISTER
Ff = OUTPUT OF COMPENSATION FLIP-FLOP.
HC = OUTPUT OF COMPENSATION CARRY FLIP-FLOP.

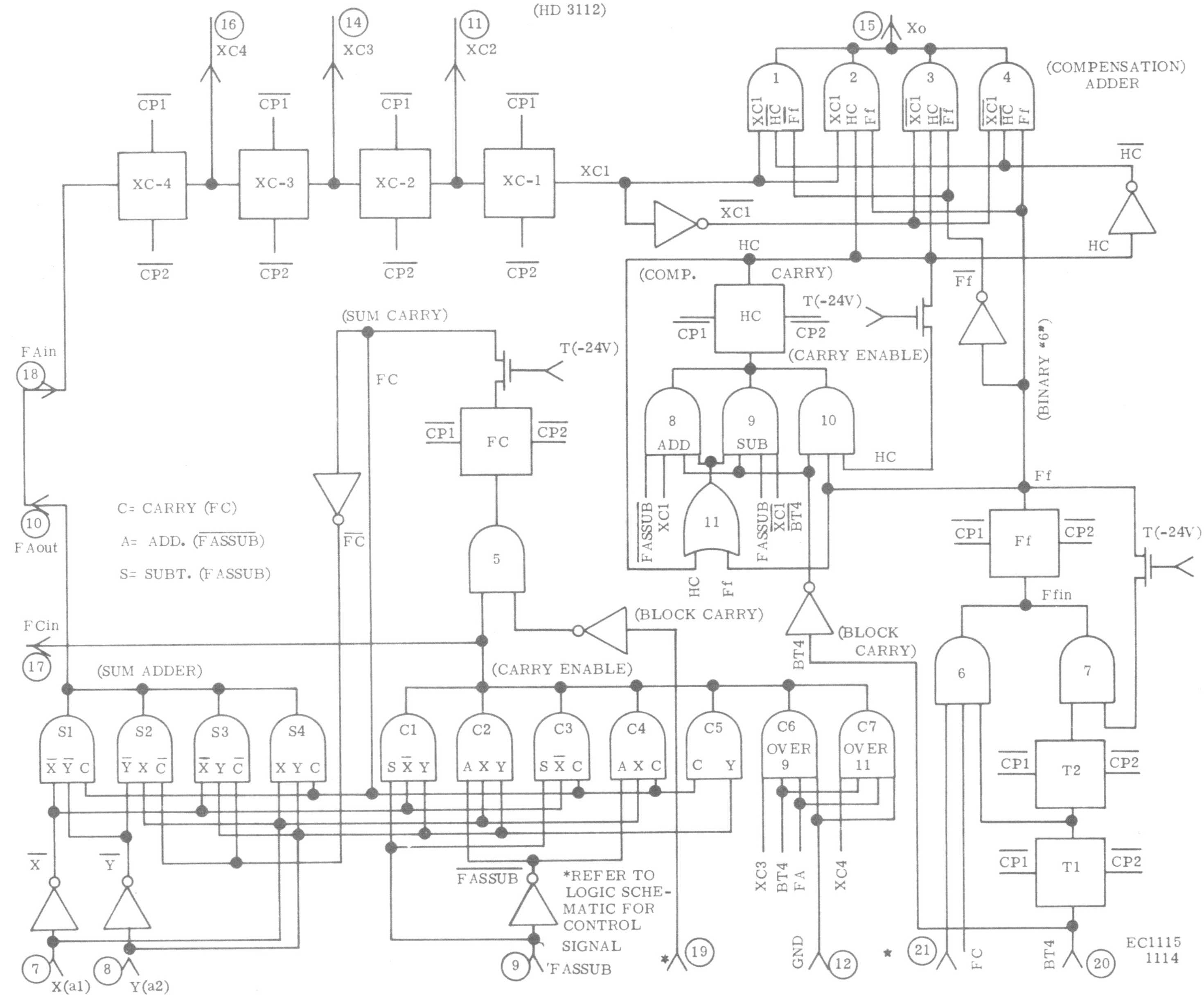
XO = COMPENSATION ADDER OUTPUT
HC ENABLE = CARRY ENABLE INPUT AT $\overline{BT4}$. (NOTE: CARRY CANNOT BE ENABLED AT BT4 TIME.)

7. HD 3112 (Delayed Full Adder)

This IC is a Medium Scale Integrated Circuit (MSI) and performs as a series delayed Full Adder/Subtracter. Figure 3-8 shows the HD 3112 IC as it is used in the EC 1115 machine. (FAS Add and Subtract Truth Tables are illustrated on page 3-4.)

FULL ADDER & SUBTRACTER

(HD 3112)



HD 3112

FIGURE 3-8

8. HD 3115 (RSS Flip-Flop)

This MOS IC contains 3 RSS type flip-flops so designated because of the set-reset control logic which acts in the following manner.

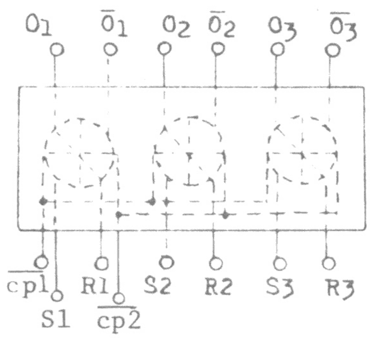
(1) With a false input to the set and reset inputs, the output of the FF does not change when triggered.

(2) With a false input to the set input and a true to the reset input, the FF will transition to the reset (true) condition when triggered.

(3) With a true to the set input and a false to the reset input, the FF will transition to the set (true) condition when triggered.

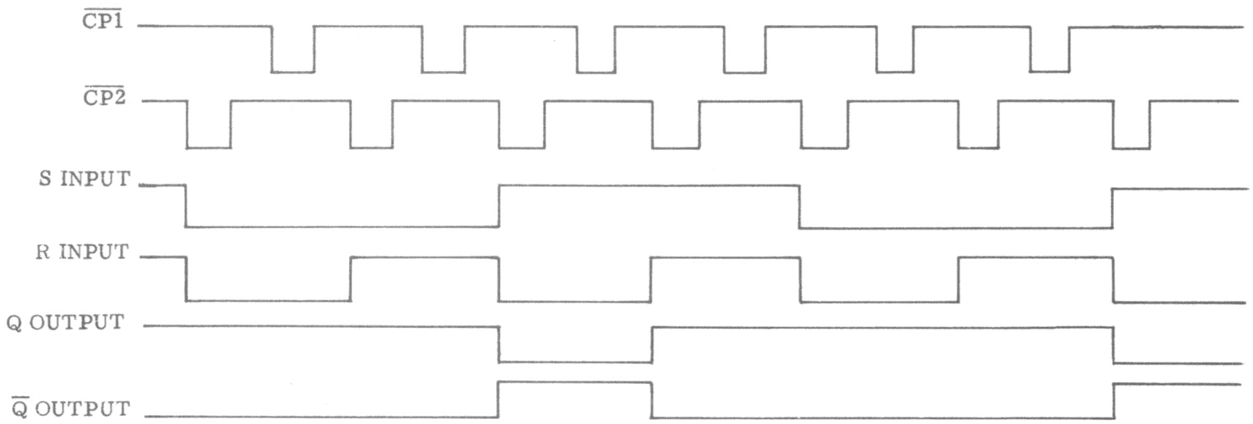
(4) With a true at both the set and reset inputs, the FF will set if it was reset, but it does not toggle under this condition.

The IC is shown in the diagram (Figure 3-9) below, along with its truth table.



logic table for R-S-S flip-flop

INPUT		SET SIDE OUTPUT
S	R	O
0	0	Qn (NO CHANGE)
0	1	0
1	0	1
1	1	1

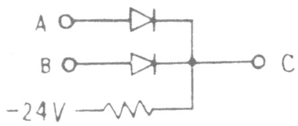


HD 3115

FIGURE 3-9

9. OR GATE

OR gates in this machine are composed of discrete components (diodes) arranged as shown in the illustration below (Figure 3-10). (NOTE: Diode packs (HD9001) containing 4 diodes are also used.)



OR GATE

A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

"OR" TRUTH TABLE

FIGURE 3-10

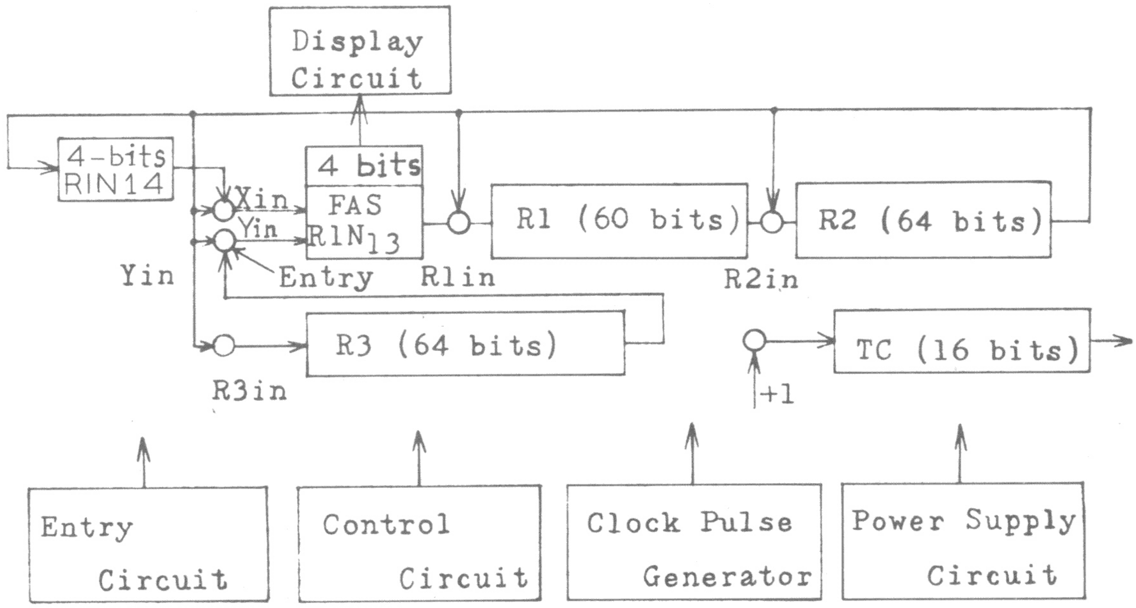
SECTION 4

FUNCTIONAL DESCRIPTION

SECTION CONTENTS

A. GENERAL

In Figure 4-1 is shown a block diagram of the 1115 Electronic Calculator indicating the data flow through the registers. A brief explanation of the block diagram and associated control circuits is included here to aid in understanding the operation of the machine.



1115 BLOCK DIAGRAM

FIGURE 4-1

FAS: Full Adder/Subtracter (includes R1N13 consisting of 4-Bits).

R1N14: 4-Bits of R1 Register used only in a left shift operation.

R2: Entry input and output (answer). Also used in series with R1 for dynamic data flow and during calculation to develop the answer in conjunction with the other two registers (R1 & R3) and FAS. (64 bit dynamic shift register.)

R3: Factor Register (64 bit dynamic shift register).

TC: Counter (16 bit static shift register).

B. OPERATION OF EACH REGISTER

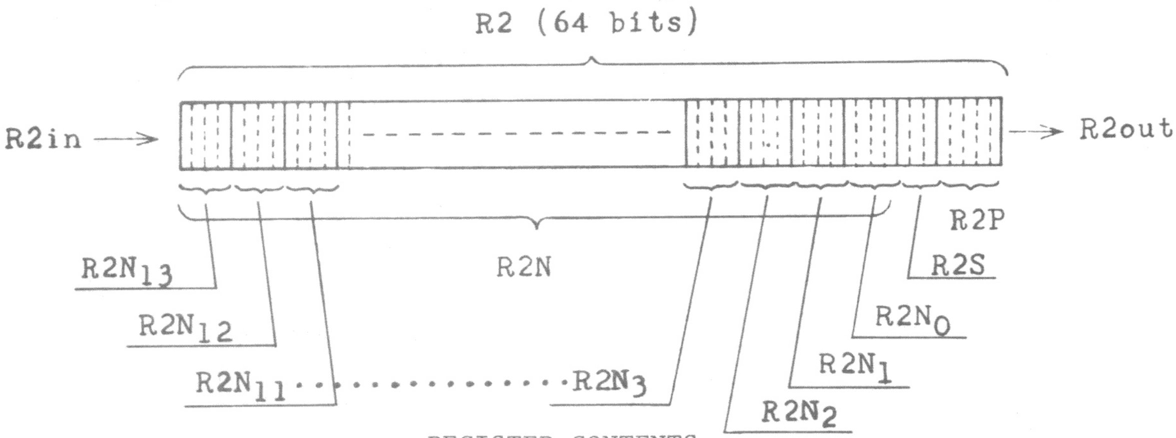
Each register stores data in a unidirectional shift flow. That is, data flow is dynamic and serial in the form of binary coded decimal (BCD) information. Data is organized into Word times, Digit times, and Bit times under control of the clock pulses: CP1 $\overline{\text{CP1}}$. $\overline{\text{CP2}}$, $\overline{\text{BT4CP1}}$, $\overline{\text{WTCP1}}$, and $\overline{\text{WT2CP1}}$.

B. OPERATION OF EACH REGISTER (Cont.)

Entry data and the result (output) is retained in R2 and the output data from R2 is gated into the input of R2 to form a loop. At the same time that R2 data is re-circulated into its own input gate, it is parallel shifted into the Full Adder and Subtracter (FAS). Then the BCD data output from FAS is gated into a decoder circuit to the Indicator Nixie Tubes for display. During the time R2 data is being displayed via the output from FAS, the data loop between FAS and register R1 is open and the contents of FAS and R1 are eliminated. However, when the machine is in a calculating operation, the output of R1 is connected to the input of R2 to form a double length register of 32 digits (128) bits. (Note: R1N14 is used only during a left shift, therefore, its output is open.)

1. REGISTER CONTENTS

In this machine, a decimal point counter and sign flip-flop are not used. Instead, the decimal point and sign information are stored within specific positions in the register. That is, each register consists of 64 bits (16 digits) and registers R2 and R3 are divided into segments having 56 bits, 3 bits, and 5 bits. The portion of the register having 56 bits is used for retaining the arithmetic data. The next portion having 3 bits is used for retaining the sign data; and the portion having 5 bits is used for retaining the decimal point data. The relative position of the 3 segments of the register is shown in Figure 4-2. Starting at the right end of the register each segment is explained as follows:



REGISTER CONTENTS

FIGURE 4-2

R2P (5 bits):	Contains information defining the decimal point position of the number to be displayed.
R2S (3 bits):	Contains the sign data which is defined as "000" for positive and "100" for for negative.
R2N (56 bits):	Contains the binary coded decimal (BCD) information representing the arithmetic data.
R2NO (4 bits):	Used when calculating a Round Off.
R2N-1∿N-12:	The contents in this position represents the 12 digits to be displayed.
R2N-13:	The 4 bits in this position are used in the dynamic data loop and also to detect an overflow condition.

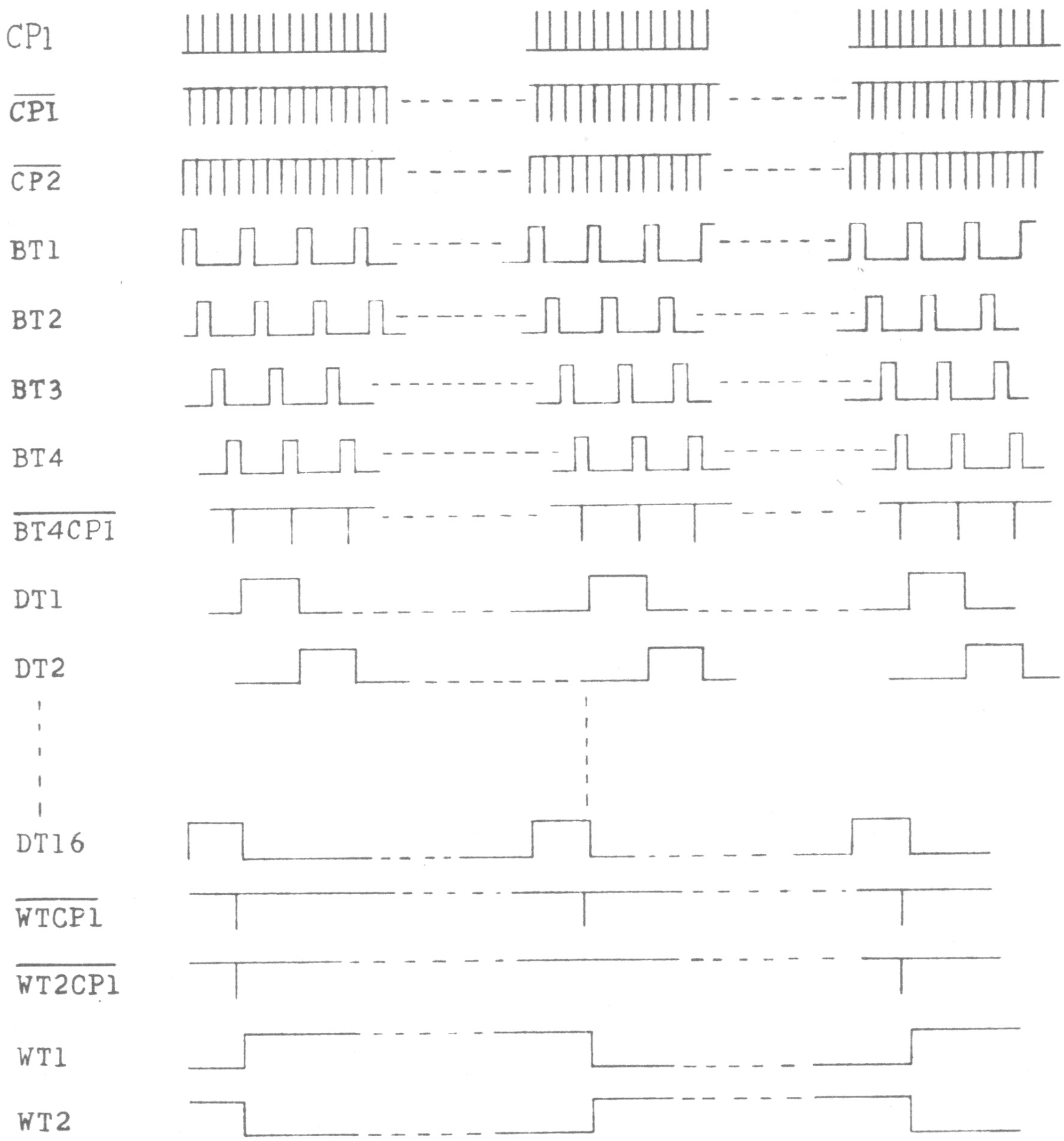
2. SHIFT PULSE AND TIMING

In this machine, the following shift pulses and timing pulses (Figure 4-3) are used.

Timing Pulse: WT1, WT2, DT1 through DT16, and BT1 through BT4.

Clock Pulses: $\overline{\text{CP1}}$, $\overline{\text{CP2}}$, $\overline{\text{BT4CP1}}$, $\overline{\text{WTCP1}}$, $\overline{\text{WT2CP1}}$, and CP1.

NOTE: WT1+WT2 is equal to one word time and there are 128 shift pulses generated during each word time. Each shift pulse corresponds to one bit time in the register.

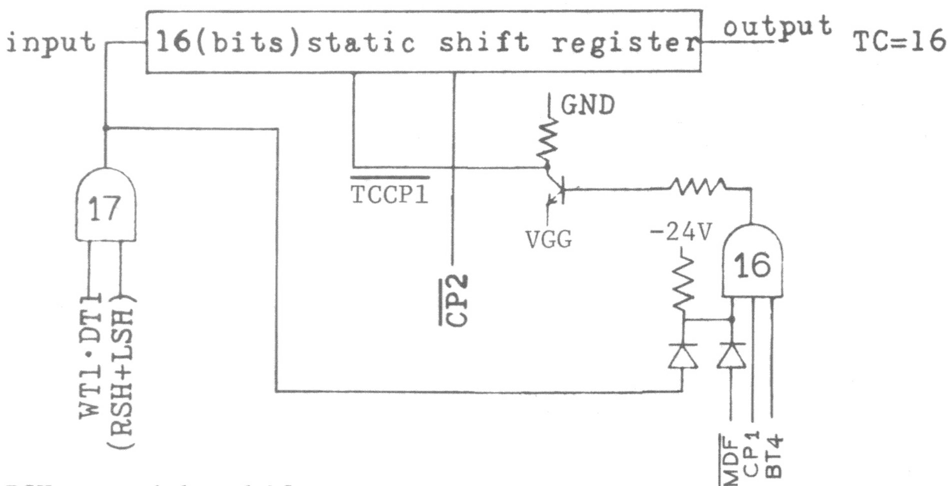


TIMING WAVEFORMS

FIGURE 4-3

3. OPERATION OF TC COUNTER

The TC Counter is a 16-bit counter (corresponding to the information in one register) used for controlling the shifting of data during a Mult or Divide operation. For example, when the MDF FF is set indicating a Mult or Divide operation the right or left shift enabling logic to Gate 17 will cause an input pulse to the TC counter each WT1.DT1 time. Also, each time Gate 17 is enabled, it enables Gate 16 and the TCCP1 shift pulse will increment the TC Counter. When a Mult or Divide operation is not being performed, Gate 17 is inhibited and Gate 16 is enabled via the signal $\overline{MDF}$, therefore, the TC Counter will be cleared.



RSH : right shift

LSH : left shift

$\overline{MDF}$: output in multiplication and division

TC COUNTER

FIGURE 4-4

C. BASIC MACHINE OPERATION

A general description of the EC 1115 operation covering the: 3-Register Calculation, Display Circuits, Input Circuits, Power Supply and Auto Clear Circuit, and Master Oscillator and Clock Pulse Generator is included in this section of the manual.

Data flow in the three registers of the 1115 is serial and dynmmic in step with the four bit times, BT1, BT2, BT3, and BT4 developed in each digit time, and under control of the clock pulses, CP1, CP2, BT4CP1, WTCP1, and WT2CP1. A complete data loop via R1 and R2 consists of 32 digits (128 bit pulses) under control of the Clock Pulse Generator.

C. BASIC MACHINE OPERATION (Cont.)

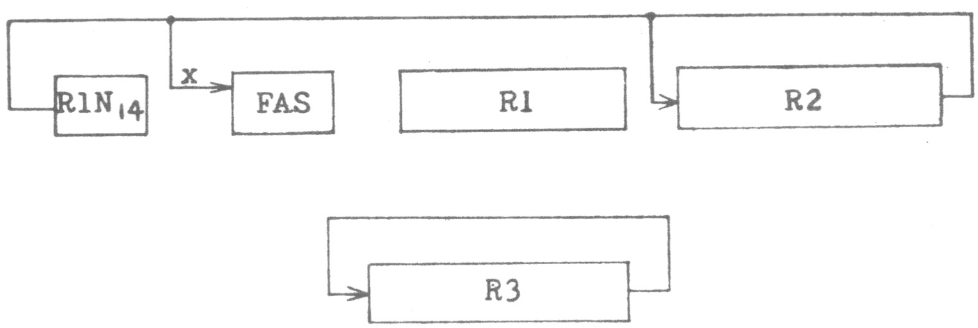
The logic for the 1115 is similar to that of the 1114 but does not include the "Underflow" system, or the "Memory" storage. It does however, operate with a 3-register system, a Roundoff Feature, an Overflow system, a Fixed Decimal Point output controlled by a Decimal Switch, a Floating Point input system, and a Constant Multiplier or Divisor feature.

1. DEVELOPMENT OF THE FUNDAMENTAL OPERATION

The fundamental operation of the 1115 concerns the data flow within the registers during the time of Display and during the time the machine is calculating. Both of these conditions will be explained in the illustrations and discussion that follow.

The fundamental operation of the 1115 can be divided as follows:

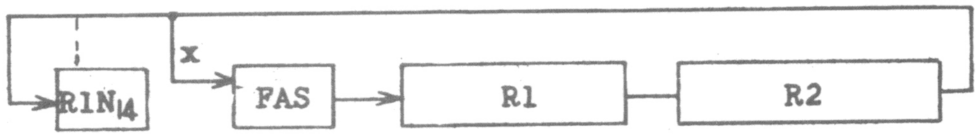
FUNDAMENTAL OPERATION
- DISPLAY CONDITION--CIRCULATION
- CALCULATING CONDITION
  - CIRCULATION
  - RIGHT SHIFT
  - LEFT SHIFT
  - EXCHANGE
  - ADD or SUB

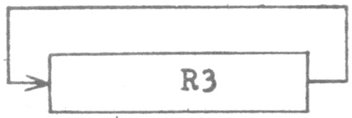


DISPLAY CONDITION--CIRCULATION

FIGURE 4-5

a. DISPLAY CONDITION--CIRCULATION. In a display condition without key operation (machine idling), the data movement throughout the 3-registers is as shown in Figure 4-5. Output data from register R2 re-enters the input to R2 and at the same time it enters the "X" input to the full adder and subtracter (FAS). The Xo output between FAS and the R1 register is open and the FAS Xo output data is destroyed. The display outputs from FAS (FA, XC2, XC3, and XC4), however, are used to feed the display decoder circuits and therefore, R2N data is displayed digit by digit as it enters FAS. The contents of R2 and R3 are retained in their closed loops, making two complete circulations each word time.



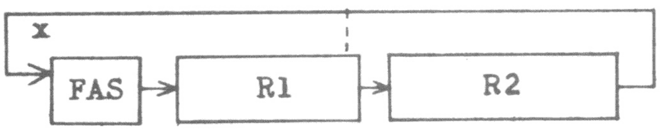


CALCULATING CONDITION --CIRCULATION

FIGURE 4-6

b. CALCULATING CONDITION--CIRCULATION. In a calculating condition, the circulation when not doing a right or left shift, exchange, or add or subtract function is as shown in Figure 4-6. During this circulation, the Xo output between FAS and R1 is closed, allowing data flow through R1, R2, and FAS in a circulatory loop. The contents of register R3 are retained via the closed loop and two circulations of R3 are completed during one circulation of R1-R2-FAS. During the time R1-R2-FAS is circulating, the contents are being sensed in order to determine the next step of the function being performed.

RETAIN POSITION

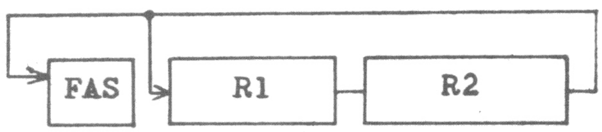


(WT1.DT1.DT2.DT3)

DEC.INFO.--SIGN--ROUNDOFF

Route of R2P.R2S.R2N during DT1 through DT3 of WT1 time to retain the decimal and sign data in its proper position.

RIGHT SHIFT (RSH)



WT1.WT2.$\overline{DT1}$.$\overline{DT2}$.$\overline{DT3}$

RIGHT SHIFT (RSH)

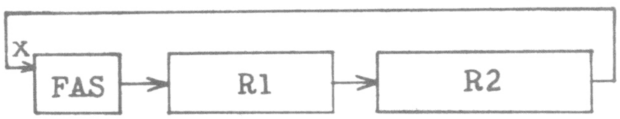
Route of calculated data during DT4 through DT16 of WT1 and WT2 to accomplish a right shift of one digit position.

RIGHT SHIFT

FIGURE 4-7

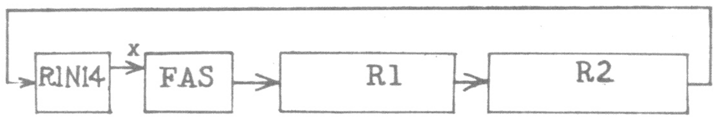
c. RIGHT SHIFT (RSH). As mentioned previously, register R2 is divided into data segments designated R2N, R2P, and R2S with each segment retaining calculated data, decimal point data, and sign data respectively. In a right shift operation, the calculated data is shifted one digit position to the right. Since R1 is used for retaining the entire calculated data, the contents of R1 and R2N must be shifted at the same time. On the other hand, since the contents of R2P and R2S must be retained without shifting data positions, the data in these two segments is routed in a different circulatory loop than the calculated data. The routing and timing for the two conditions is shown in Figure 4-7.

RETAIN POSITION



Route of R2P.R2S.R2N during DT1 through DT3 of WT1 time to retain the decimal and sign data in its proper position.

LEFT SHIFT

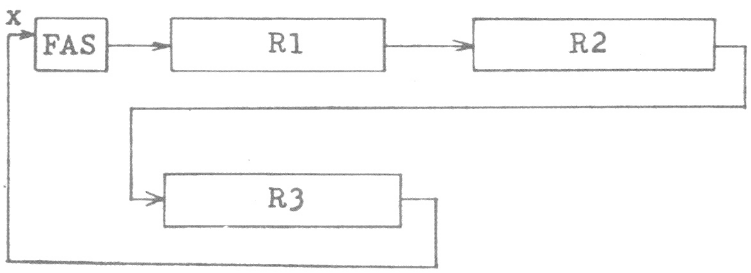


Route of calculated data during DT4 through DT16 of WT1 and WT2 to accomplish a left shift of one digit position.

LEFT SHIFT

FIGURE 4-8

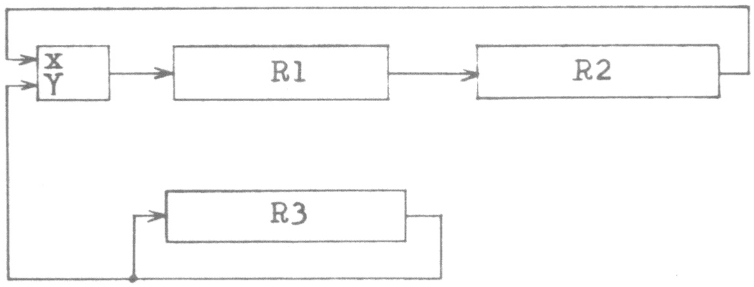
d. LEFT SHIFT (LSH). In a left shift operation, the contents in R1 and R2N are shifted one digit position to the left, but the contents in R2S, R2P, and R2N-0 are retained in their respective positions. That is during DT1 through DT3 time, the contents of R2P, R2S, and R2N-0 are circulated in the data loop via the normal idle shift route. Then, during DT4 through DT16 time, of WT1 and WT2, the contents of R1 and R2N are routed into R1N-14 to cause a left shift. The routing and timing for the two conditions is shown in Figure 4-8.



EXCHANGE

FIGURE 4-9

e. EXCHANGE (CHG). In an exchange operation, the contents of R2 (R2N, R2P, and R2S) are exchanged with the contents of R3 (R3N, R3P, and R3S) during WT1 time (1st half of the word time). The routing of the registers is shown in Figure 4-9.

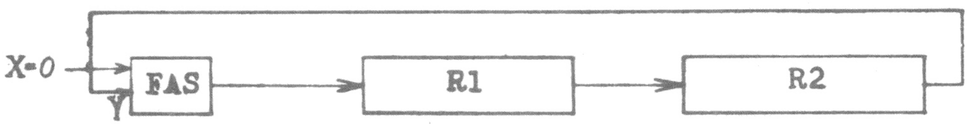


The Timing of Y-input	Operation	Calculation
DT3∿DT16 of WT1	R2N±R3N	Addition & subtraction
DT3∿DT16 of WT2	R1±R3N	Multiplication & division

ADD OR SUBTRACT

FIGURE 4-10

f. ADD AND SUBTRACT (AOS). In an Add or Subtract operation, the contents of R2N and R3N, or R1 and R3N are gated into the full adder and subtracter FAS and the sum or difference of the two factors is developed. The composition of registers in R1±R3N and R2N±R3N is the same, but the two calculations are distinguished from each other by the timing into the "Y" input of FAS. For example, as shown in the chart below Figure 4-10, the timing of the "Y" input to FAS for an Add or Subtract operation of R2N+R3N occurs in DT3 through DT16 of WT1. The timing of the "Y" input for a Mult or Divide operation of R1±R3N occurs in DT3 through DT16 of WT2.



DT3 through DT16 of WT1

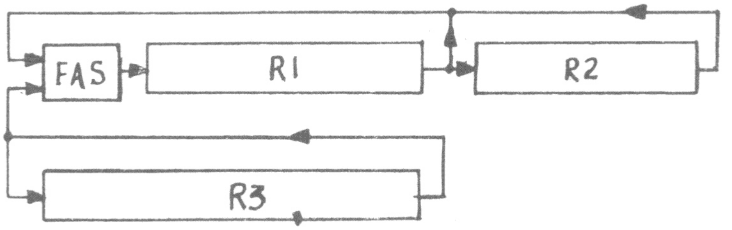
CHANGE TO AND FROM COMPLEMENT

FIGURE 4-11

g. COMPLEMENT (CWF). In addition and subtraction, the contents of R2N circulates via the "Y" input to FAS during one word time after the Add or Subtract function. Then, if the result (output) of a subtract operation is a complement, another subtract command is given to FAS and the contents in R2N is subtracted from "0" changing the complement to a positive number. The routing of the CWF operation is shown in Figure 4-11.

2. THREE REGISTER OPERATION

As shown in Figure 4-12, three registers designated: R1, R2, and R3 are used in conjunction with the Full Adder and Subtracter (FAS) to perform the arithmetic calculations. The three register system is explained briefly as follows:

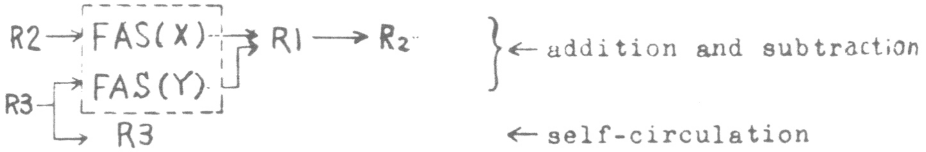


FAS: FULL ADDER AND SUBTRACTER

FIGURE 4-12

a. ENTRY DATA is gated into R2 and the previous answer or data already in R2 is shifted into R3. As data circulates through the route of R1-R2-FAS-R1, the contents of R3 make two passes through its data loop.

b. ADD OR SUBTRACT. In an Add or Subtract operation, the arithmetic calculation is performed between the contents of R2 and R3 as shown in the data flow diagram, Figure 4-13.



ADD OR SUBTRACT

FIGURE 4-13

c. MULT. In a Mult operation, R2 contains the multiplier and R3 contains the multiplicand. A series of repeat "Add" operations are carried out for each digit, and the partial product is gated into R1. As each repeat "Add" cycle is completed for each digit, a control number in R2 is decremented by "1" until it reaches "0", and then a right shift occurs to bring the next control digit into position for the next series of repeat "Add" cycles. As the product is developed (partial product) it is fed into R1 and R2 in series. At the end of the mult operation, the final product is in R2.

d. DIVIDE. In a Division operation, R2 contains the dividend and R3 contains the divisor. A series of repeat subtractions (R1 - R3) is performed until an overdraft occurs. As each subtraction is performed, R2N1 is incremented. The overdraft is then restored, R2N1 is decremented, and the data in R1 and R2 is shifted left one digit position. This sequence of: repeat subtraction, increment R2N1, restore overdraft, decrement R2N1, shift R1 and R2 left is performed as part of the answer development. The successful subtractions are incremented in R2N1 each time until an overdraft occurs, signaling the start of the "restore overdraft", decrement R2N1, left shift cycle. This action will continue until the quotient in R2 has shifted left so that its MSD is in the R2N13 position. At this time, the final decimal alignment of the quotient begins with R2 shifting right until the number of decimal places in the quotient is equal to the setting of the decimal switch.

e. 3-REGISTER CALCULATION USING EXAMPLES. To aid in understanding the machine operation, a brief description of an "Add" operation and a "Mult" operation is included here.

(1) Addition (Decimal Switch on "5")

Example: 1.23 + 45.6 = 46.83000

(a) Entry of 1.23

1. Depression of the digit key "1" causes the contents of the R2 register to be shifted to R3 and a binary coded decimal 1 (0001) to be entered into the LSD position of R2 (R2N1).

2. Depression of the decimal point key causes the decimal point control flip-flop (POT) to set.

3. Depression of the digit key "2" causes the contents of register R2 to shift left one digit position while the new entry "2" is shifted into the LSD position of R2. Also, at the time the "2" is being entered, a "1" is added to the decimal point information in R2P.

4. Depression of the digit key "3" causes the same action as described for the digit key "2".

At the end of the entry of 1.23, the contents of the registers appears as shown in Figure 4-14.

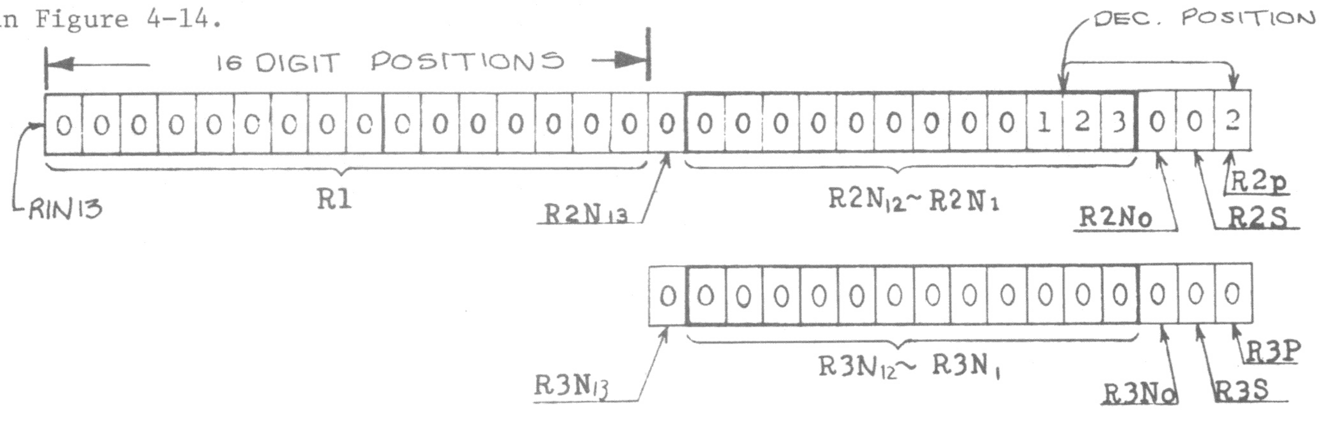
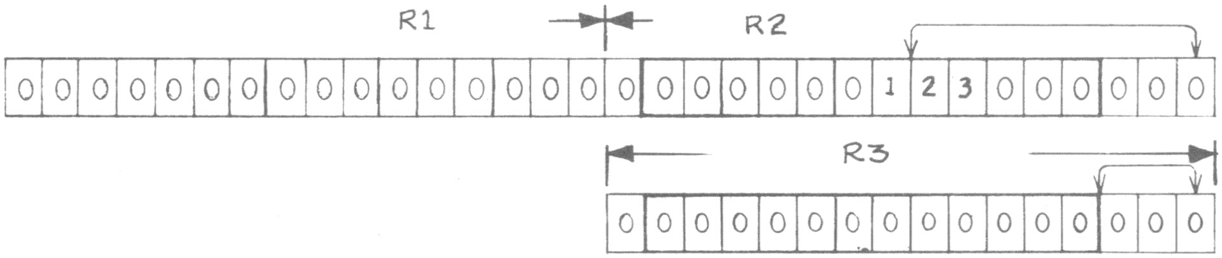


FIGURE 4-14

(b) Function Key Operation (+=). Depressing the Plus Equal key causes the following actions:

1. Alignment. The number of decimal point digits of the contents "1.23" of R2 (retained in R2P) is compared with the decimal preset number "5". Since the contents of R2P are smaller than the decimal point number, the contents of R2N are shifted to the left a number of places equal to the difference between R2P and the decimal preset number and R2P is incremented by "1" for each left shift.

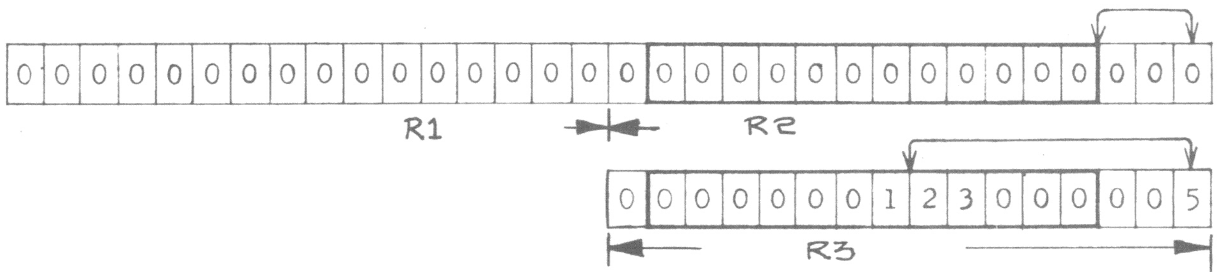
In this example, after the above alignment operation, the contents of R2N becomes: 1.23000 and the contents of R2P becomes: "5". The contents of the registers are as shown in Figure 4-15.



ALIGNMENT

FIGURE 4-15

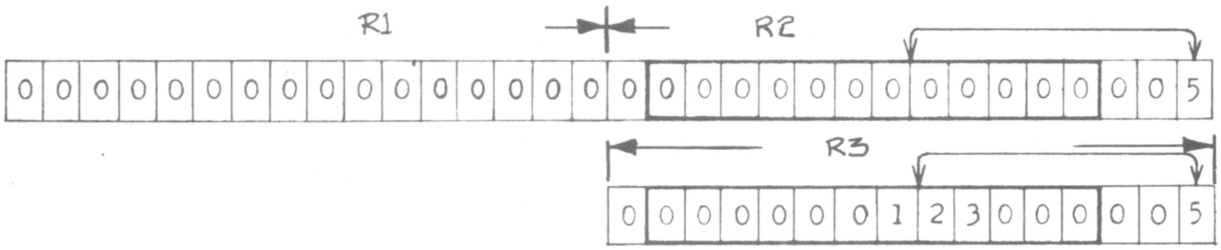
2. Exchange. Depression of the Plus Equal key causes the R2 contents "1.23000" to be exchanged with the contents of R3 and the register appears as indicated in Figure 4-16.



EXCHANGE

FIGURE 4-16

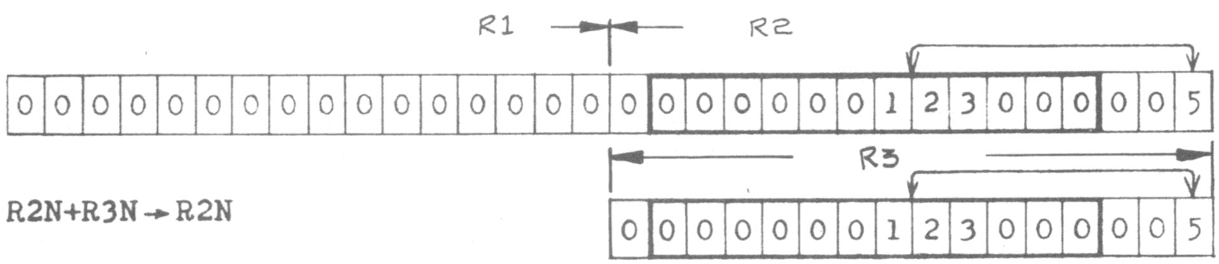
3. Alignment. After the exchange operation takes place as described in item 2, another decimal alignment takes place the same as described in item 1. Then, as shown in Figure 4-17, the contents of R2 becomes "0.00000" by shifting five digit positions to the left; and the contents of R2P becomes "5" as a result of the five left shifts.



ALIGNMENT

FIGURE 4-17

4. Addition. The contents of R2N "0.00000" and the contents of R3N "1.23000" are simultaneously gated into the Adder (FAS) and the added output is gated into R2N. The contents of R3N are retained in R3N. As a result, the number 1.23000 is retained in R2 and R3 as shown in Figure 4-18.

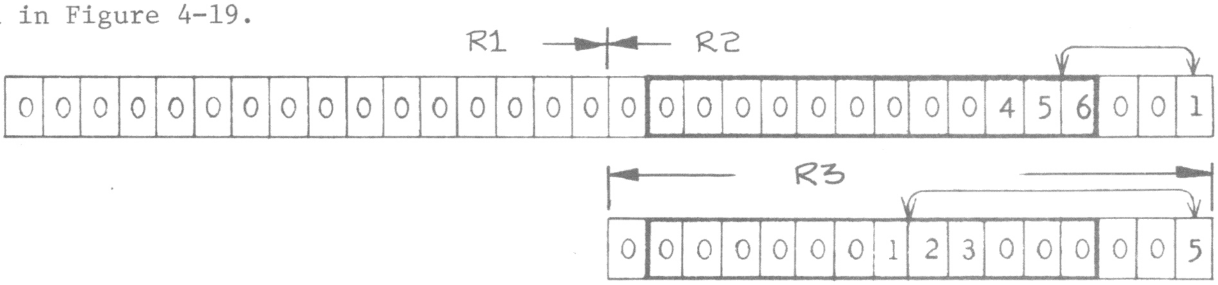


ADDITION

FIGURE 4-18

5. Round Off. A round off, if desired, is done during the final steps of the calculation. For example, if the R/0 key is latched down and the contents of R2N-0 are larger than "4", a "1" is added to the LSD of the number displayed in R2. The R2N-0 contents are then cleared in readiness for the next calculation.

(c) Entry of 45.6. Entry of the digits 45.6 is accomplished in the same manner as described for the entry of 1.23. The contents of the register after entry are as shown in Figure 4-19.



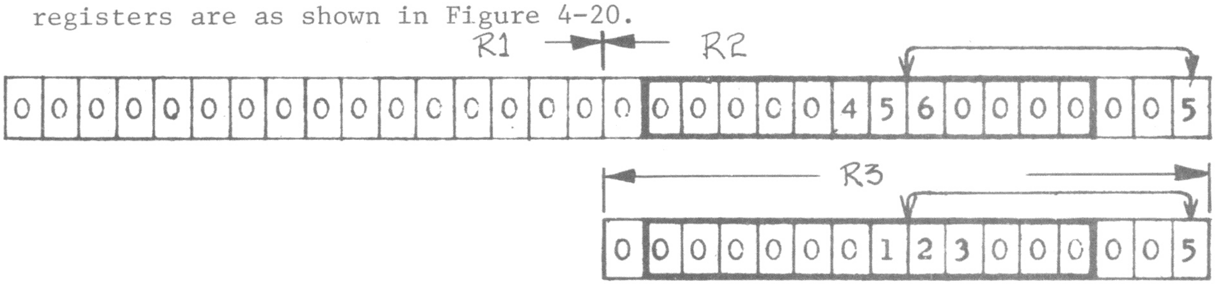
ENTRY

FIGURE 4-19

(d) Function Key Operation (+=). Depressing the Plus Equal key causes the following actions to occur.

1. Alignment. The number of decimal point digits of the contents 45.6 of R2 (contained in R2P) is compared with the decimal preset number "5". Since the contents of R2P are smaller than the decimal point number, the contents of R2N are shifted to the left a number of places equal to the difference between R2P and the decimal preset number, and R2P is incremented by "1" for each left shift.

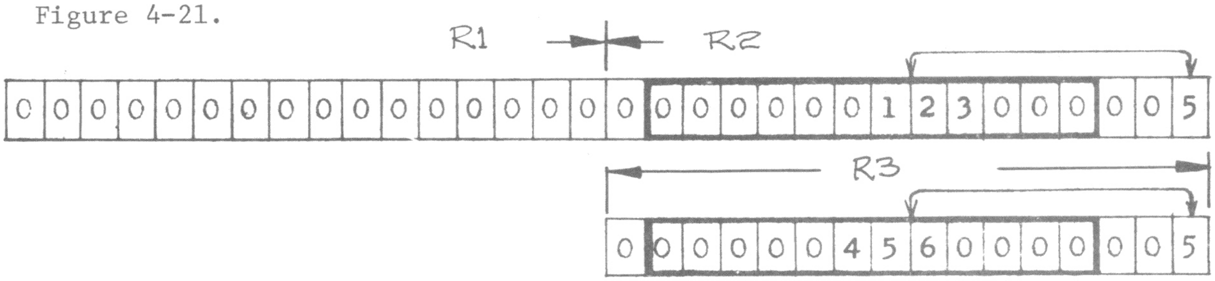
   In this example, after the alignment takes place, the contents of R2N becomes: 45.60000 and the contents of R2P becomes: "5". The contents of the registers are as shown in Figure 4-20.



ALIGNMENT

FIGURE 4-20

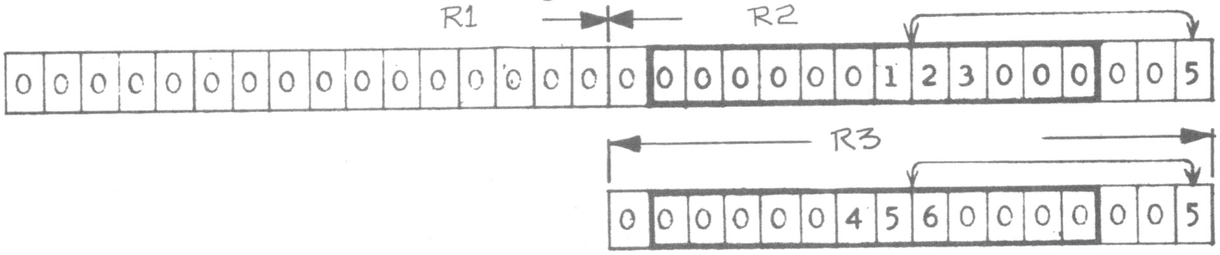
2. Exchange. Depression of the Plus Equal key causes the R2 contents 45.60000 to be exchanged with the contents of R3 and the registers now appear as shown in Figure 4-21.



EXCHANGE

FIGURE 4-21

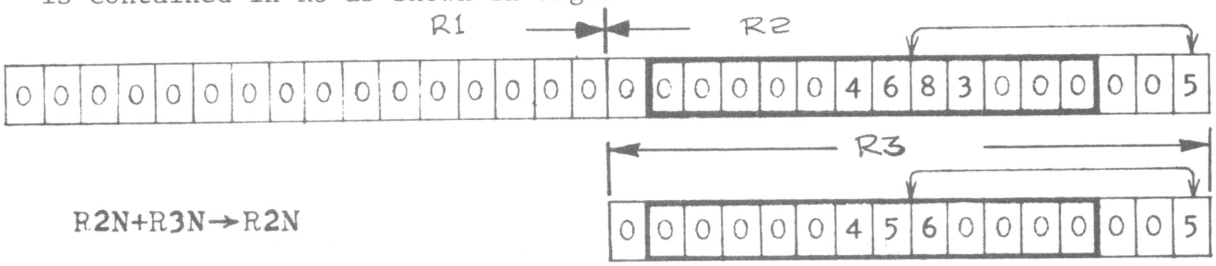
3. Alignment. After the exchange takes place as described in item 2, if a decimal point alignment is necessary it occurs in the same manner as described in item 1. The contents of the registers are now as shown in Figure 4-22.



ALIGNMENT

FIGURE 4-22

4. Addition. The contents of R2N "1.23000" and the contents of R3N "45.60000" are simultaneously gated into the Adder (FAS) and the added output is gated into R2N while the contents of R3N are retained in R3N. As a result of the addition, the number "46.83000" is contained in R2 and the number "45.60000" is contained in R3 as shown in Figure 4-23.



ADDITION

FIGURE 4-23

5. Round Off. A round off if desired, is done during the final steps of the calculation. For example, if the R/O key is latched down and the contents of R2N-0 are greater than "4", a "1" is added to the LSD of the number displayed in R2. The R2N-0 contents are then cleared in readiness for the next calculation.

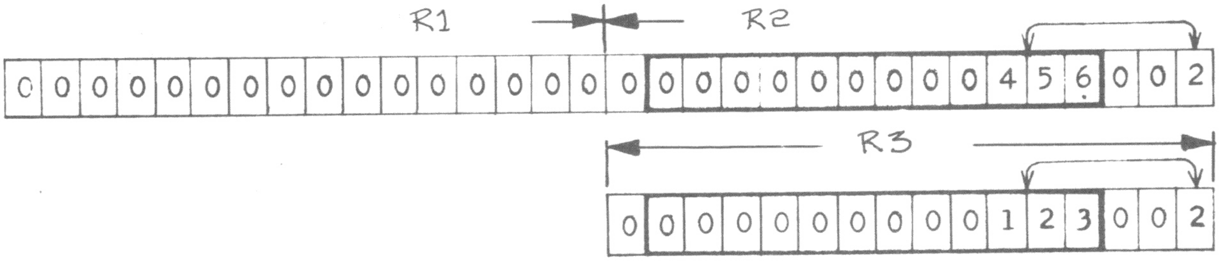
(2) Multiplication (Decimal Switch on "2")

Example: 1.23 x 4.56 = 5.60

(a) Entry of 1.23. Same as described for the Addition operation.

(b) Function Key Operation (Mult key). The control flip-flop MLT1 is set for the purpose of retaining the Mult instruction during the mult operation.

(c) Entry of 4.56. Entry of the second number "4.56" is the same as described for the second number in Addition. The contents of the registers are as shown in Figure 4-24.

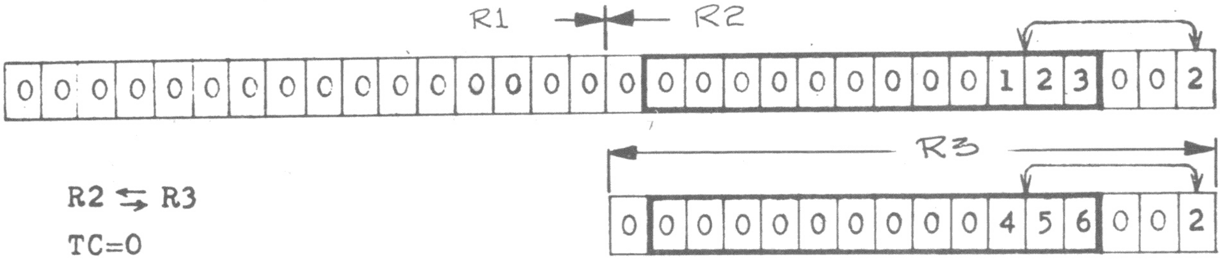


ENTRY

FIGURE 4-24

(d) Function Key Operation (+=). Depressing the Plus-Equal key causes the following actions to occur.

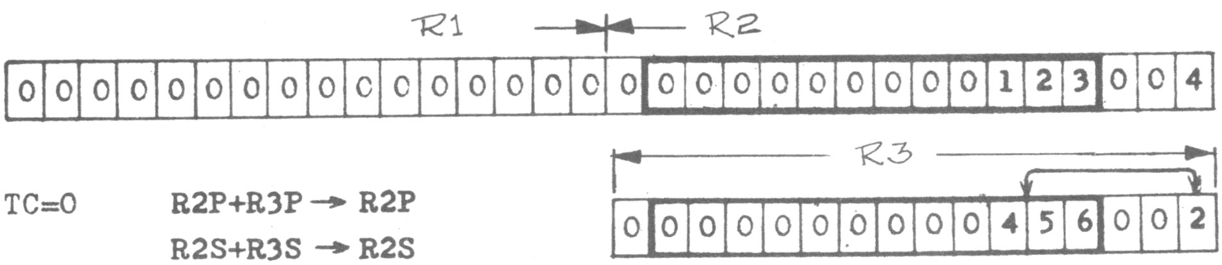
1. Exchange. The contents of R2 "4.56" are exchanged with the contents of R3 "1.23". The contents of the registers after the exchange are as shown in Figure 4-25.



EXCHANGE

FIGURE 4-25

2. Calculating the Decimal Digits and Sign of the Product. The contents of R2P (digit 2) and the contents of R3P (digit 2) are simultaneously gated into the Adder (FAS) and the added output is gated through R1 and into R2P while the contents of R3P are retained in R3P. The contents of R2P now contains a "4" which is the intermediate decimal position of the product. Also, the contents of R3S and R2S are added via FAS and their added output is gated through R1 and into R2S as the proper sign of the product. If the number in R2S is "000" after the addition, the sign is positive. If the number in R2S is "100" the sign is negative. The contents of the registers are as shown in Figure 4-26.



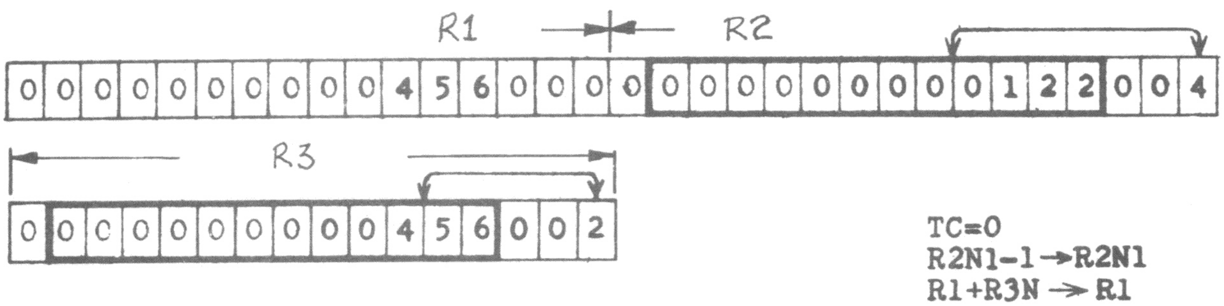
DECIMAL & SIGN

FIGURE 4-26

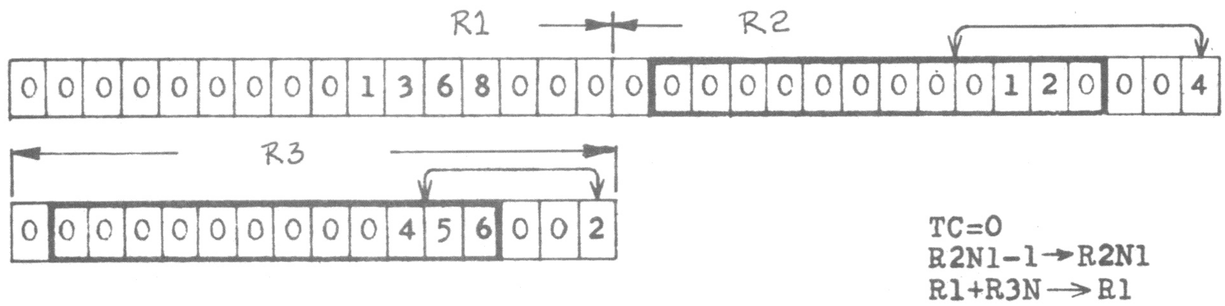
3. Repeat Addition (Mult). If the LSD of the Multiplier in R2N1 is not zero, then each subsequent data pass will add the Multiplicand in R3N to the contents of R1N, and subtract "1" from the LSD of R2N1 until it reaches zero. When the LSD in R2N1 reaches zero, the contents of R1N and R2N will be shifted right one digit position, and the TC counter will be incremented by "1" to keep count of the right shifts. This action continues for each LSD of the Multiplier until all the digits in the Multiplier have been counted to zero. When the TC counter equals 16 (TC=16) the answer will have been developed and shifted from R1N to R2N.

As a result of the Repeat Addition (Mult), the product "5.6088" is retained in register R2 and the multiplicand "4.56" is retained in R3. The series of Repeat Add cycles and right shifts are illustrated in the register diagrams, Figure 4-22.

Repeat-Addition (1 - 1)

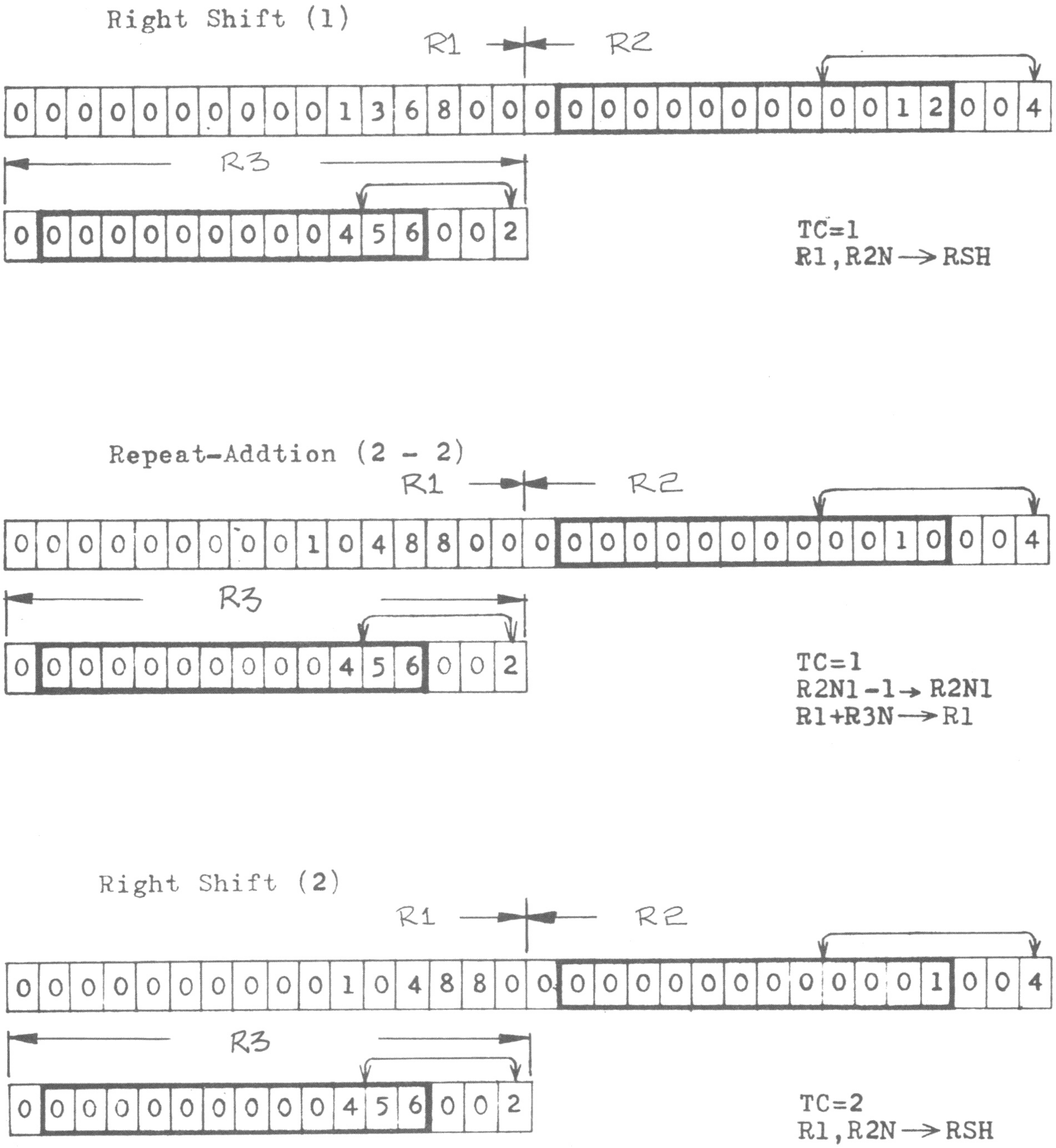


Repeat-Addition (1 - 3)



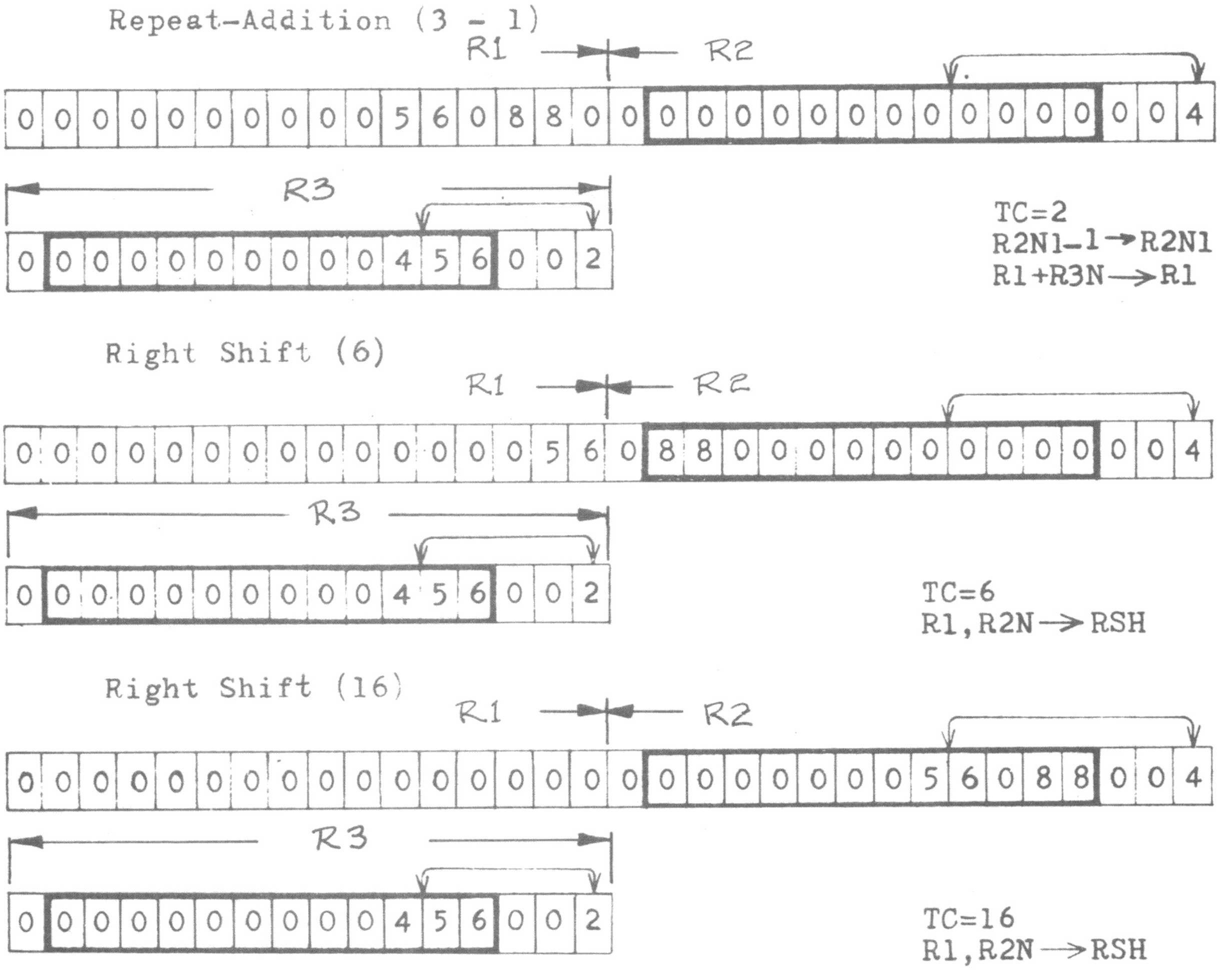
REPEAT ADD & RIGHT SHIFT
(Cont. on next page)

FIGURE 4-27



REPEAT ADD & RIGHT SHIFT
(Cont. on next page)

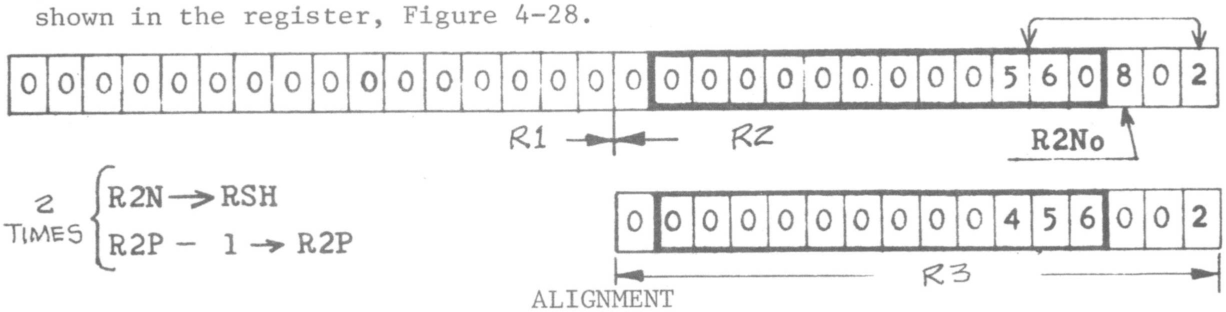
FIGURE 4-27



REPEAT ADD & RIGHT SHIFT
(Cont. on next page)

FIGURE 4-27

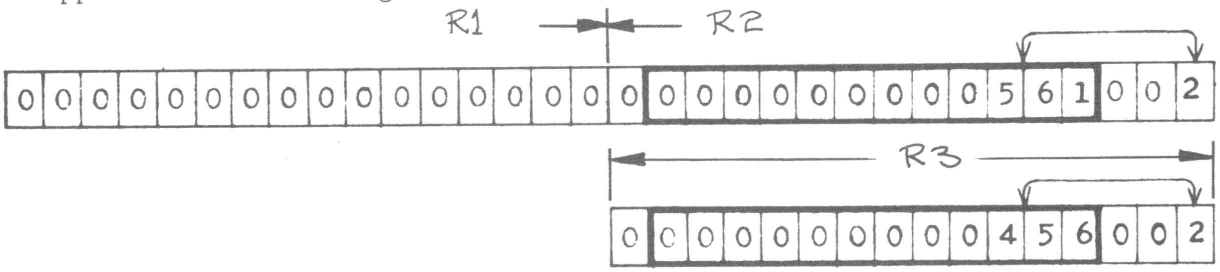
4. Alignment. The number of decimal digits of the product in R2P ("4" in this example) is compared with the decimal preset number "2" and if the number of decimals of the product is larger than the decimal preset number, the contents of R2N are shifted right a number of places equal to the difference. As each right shift occurs, a "1" is subtracted from R2P. The result of aligning the product to the position designated by the setting of the Decimal Switch is as shown in the register, Figure 4-28.



ALIGNMENT

FIGURE 4-28

5. Round Off. If the Round Off switch is latched down and the digit in R2N-0 is larger than "4", a "1" is added to the LSD in R2N. After the operation, the contents of R2N-0 are cleared. The contents of the registers after Round Off appear as shown in Figure 4-29



ROUND OFF

FIGURE 4-29

3. DISPLAY

The Indicator Circuit corresponding to the output device of a calculator consists of Indication Flip-Flops, a Logic Decoder, and Numeric and Decimal Point Indicator Drive circuits for the Anodes and Cathodes of the Indicator (Nixie) Tubes.

The Cathodes in each Indicator (Nixie) tube corresponds to the "0" through "9" digits, and the Decimal Point. Also, each tube has one Anode which is common to the Numeric and Decimal Point Cathodes. In order to fire a tube and display a particular digit (or decimal point), the Cathode associated with the digit or decimal point must be at the proper bias voltage with respect to the Anode voltage.

Decimal and numeric data is fed via the FAS outputs (FA, XC4, XC3, and XC2) to the Indicator flip-flops at the end of the digit times and is decoded via a diode decoder network. The 12 Indicator Tubes are fired sequentially in step with the digit times, starting with the #1 tube and Digit Time DT2. However, because of the arrangement of data in the R2 register: Sign, Decimal Point, Round Off, Numeric; with respect to the Digit Times (DT1 through DT16), the sequential timing occurs as indicated in the Display Timing Chart, Figure 4-30.

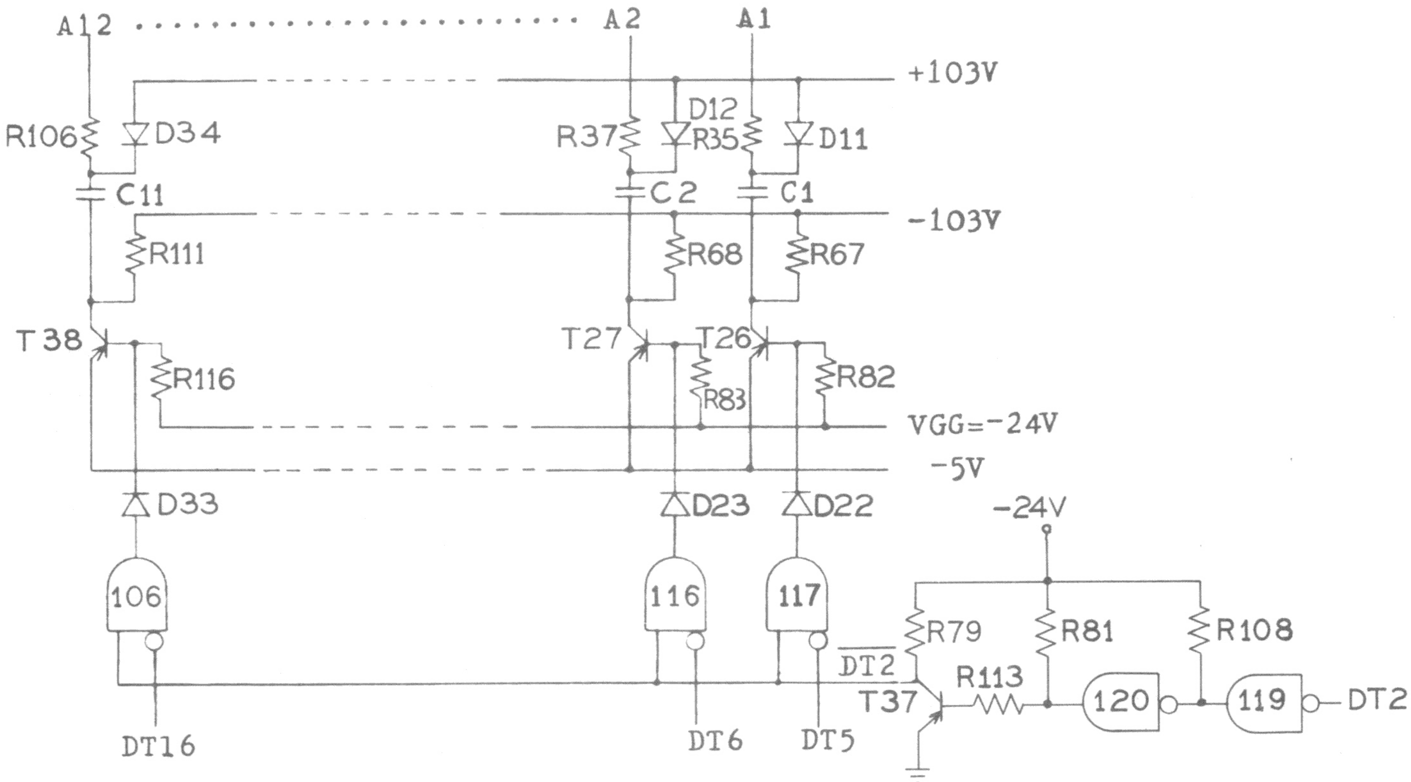
Displayed Contents	Timing	Figure to be Displayed
R2P	DT2	Decimal Point
R2N1	DT5	The 1st Figure (LSD)
R2N2	DT6	The 2nd Figure
thru		
R2N12	DT16	The 12th Figure (MSD)

DISPLAY TIMING

FIGURE 4-30

a. ANODE CONTROL CIRCUIT

A positive potential of approximately 200 volts is supplied to the Anodes of the individual Indicator Tubes in step with the associated digit time signals via their respective control circuits. This high voltage potential is developed by charging the capacitors (C1 through C11) to approximately 206 volts. Then, when an anode control transistor (T26, T27, etc.) is turned on, its collector goes to approximately -5V and the capacitor connected to its collector feels a change of 98V (-103V - 5V) in the positive direction. This +98V change on the capacitor plate is added to the +103V charge on the other plate for a total output voltage of approximately 200V to the anode of the indicator tube being fired. The simplified schematic in Figure 4-31 illustrates the charging circuit described above.



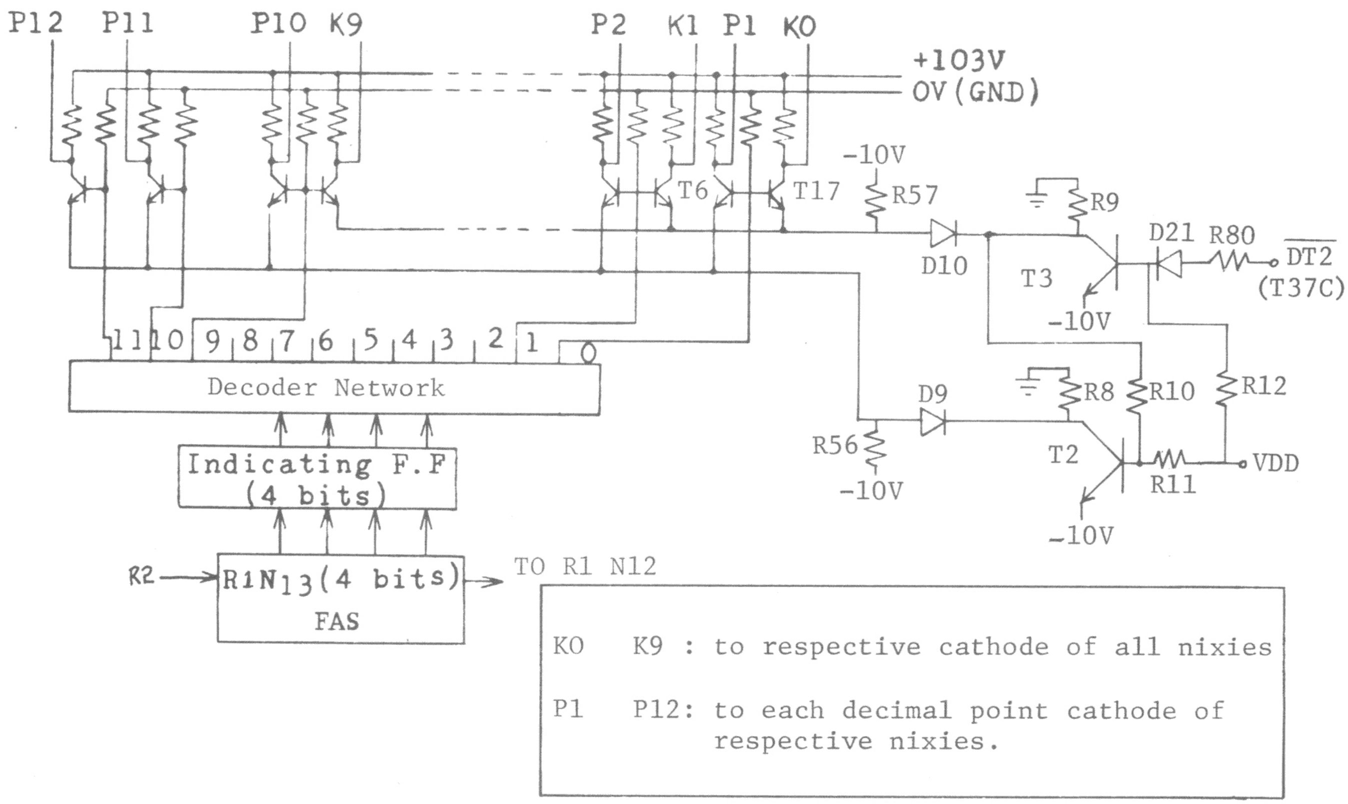
ANODE CONTROL CIRCUIT

FIGURE 4-31

In timing the firing of the Indicator Tubes, the arrangement of the data (Decimal Point, Sign, and Numeric) in the register must be considered. For example, during DT1 time, the decimal data is shifted into FAS, but during this time, the anode circuits are blocked because transistor T37 is on, clamping its collector at ground and preventing the Anode Transistors from turning on. At the end of DT1 time, the decimal point data at the FAS output terminals: FA, XC4, XC3, and XC2 is parallel shifted into the Cathode Decoder flip-flops. When DT2 goes True at the input to Gate 119, the Control Transistor T37 will turn off. With transistor T37 off, its collector output will be at logic 0 (False) and the output of all the Anode Control Gates (106 through 117) will be False, causing the Anode Driver Transistors (T26, T27, etc.) to turn on.

The Anode Driver Transistors turning on will discharge the capacitor circuits allowing approximately 200 volts to be felt at the Anodes of all 12 Indicator Tubes.

In the meantime, the transistor corresponding to the decoded Decimal Point Cathode (P1, P2, etc.) has been turned on and its collector will be clamped to approximately -10V causing the Decimal Point Cathode to glow. After DT2 time, the Anode Control Gates (106 through 117) are under control of their respective Digit Times DT5 through DT16 which corresponds to the R2-1 (LSD) through R2-12 (MSD) register positions.



CATHODE CONTROL CIRCUIT

FIGURE 4-32

b. CATHODE CONTROL CIRCUIT

Shown in Figure 4-32 are the control circuits for driving the Cathodes of the Indicator Tubes. Since there are 12 decimal point positions (P1 through P12) and 10 digits (K0 through K9), a total of 22 Driver Transistors are required. The base inputs for the digit transistors are shared with the base inputs of their respective decimal point transistors, leaving the two base inputs to the transistors for P11 and P12 independent. The emitters of the digit Driver Transistors are bused together and the emitters of the decimal point Driver Transistors are bused together; therefore, the voltage level applied to the two emitter buses will determine whether a Digit Transistor, or a Decimal Point Transistor will turn on. For example, if the data in R2P is zero, the decoder output on the "0" line establishes a turn on voltage on the bases of Transistors T17 and T6 (associated with K0 and P1 in Figure 4-32). At this same time, the control circuitry feeding the emitter buses will allow only the emitter bus connected with the decimal point transistors to forward bias the emitter for Transistor T6, causing T6 to turn on.

the emitter buses will allow only the emitter bus connected with the decimal point transistors to forward bias the emitter for Transistor T6, causing T6 to turn on.

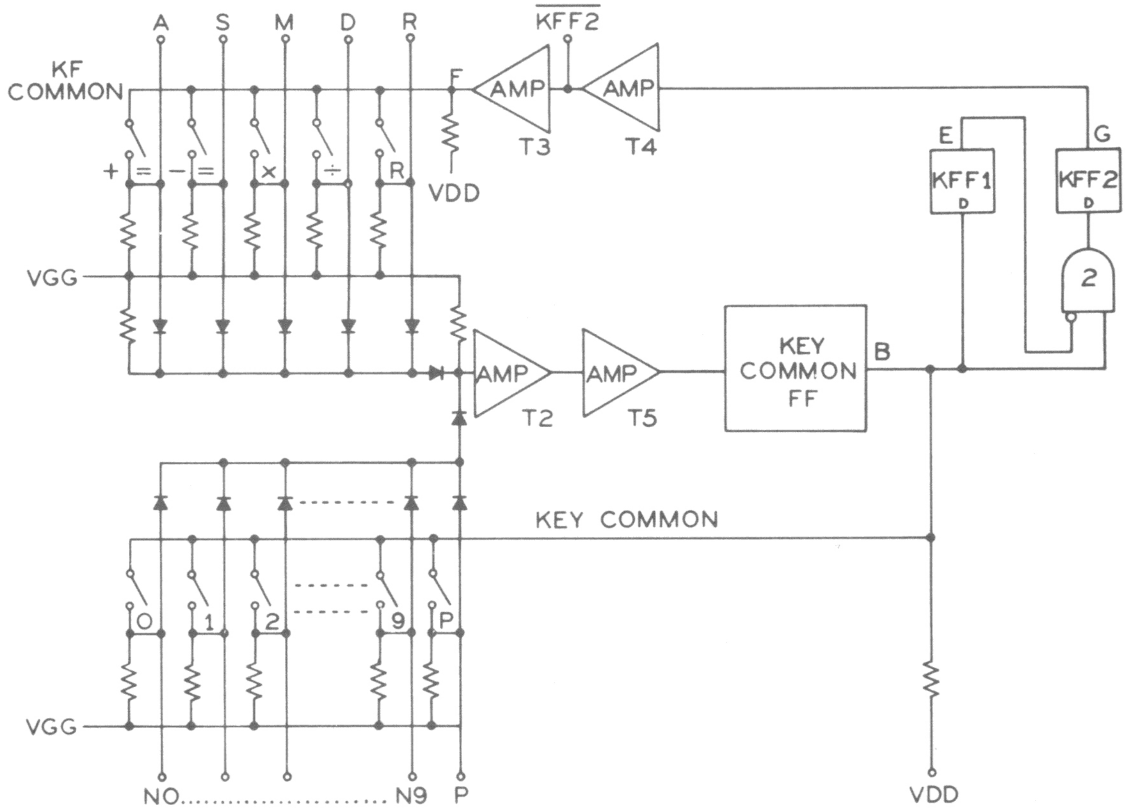
4. INPUT CIRCUITS

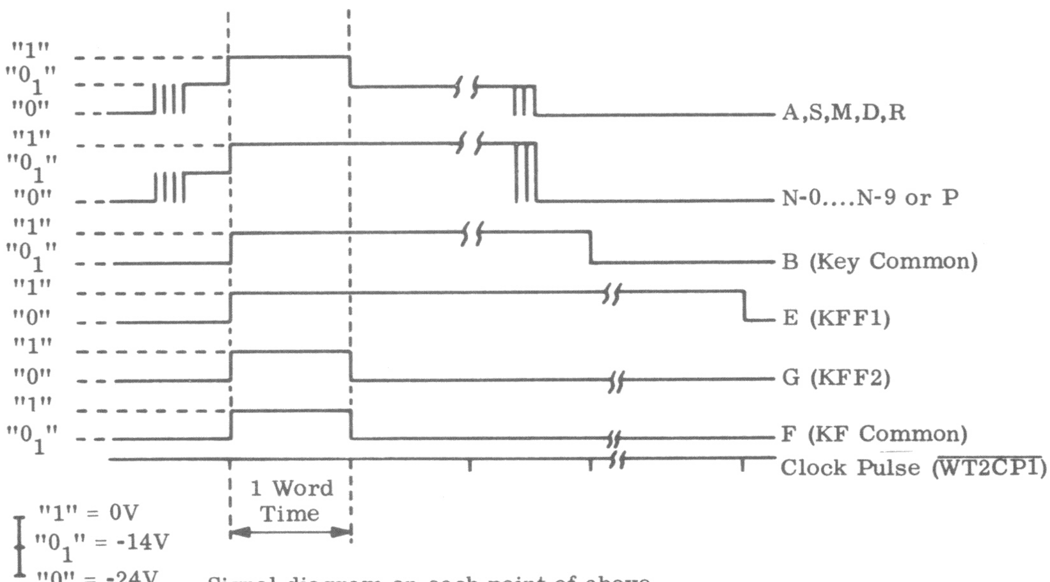
The input circuits for the 1115 machine are similar to those described for the 1114 machine in that the signal Key Common is used as the Entry Control signal and provides a time delay to ensure synchronization of all Control flip-flops to the clock pulses. The input circuits are shown in Figure 4-33.

The logic circuits controlling the 1115 machine are under control of, and synchronized with the clock pulse generator. However, Entry data developed when a digit or a function key is depressed occurs at random and must be synchronized with the machine logic. A signal designated "Key Common" is used for synchronizing the Entry data, and a signal designated "KF Common" is used for synchronizing the Function key data. Development of Key Common and KF common is described as follows:

The Key Common line and the KF Common line are initially clamped to -14 volts (logic 0) via resistor R126 at the Set input terminal of the Key Common FF, and resistor R129 at the collector of transistor T3. When a Numeral, a Decimal Point key, or a Function key is depressed, its corresponding switch is closed and the appropriate diodes in the diode decoder network are forward biased allowing transistor T2 to turn on. As transistor T2 turns on, its collector is connected to a delay circuit (RC circuit) which provides the turn on potential to transistor T5 after a period of approximately 5 milliseconds. When transistor T5 is fully on, its collector being True enables the setting of the Key Common FF and when the clock pulse WTCP1 occurs, the Key Common FF is permissed to set.

As the signal "Key Common" goes True in synchronization with the clock pulse $\overline{\text{WTCP1}}$, KFF1 and KFF2 are enabled to be set. (KFF2 set input is also qualified by the False output from KFF1.) Then, as the clock pulse $\overline{\text{WT2CP1}}$ occurs, KFF1 and KFF2 are set simultaneously. Prior to KFF2 being set, its output is False into the base of transistor T4 and T4 is off. The collector of T4 "$\overline{\text{KFF2}}$" is therefore at 0 volts (True) into the base of transistor T3 and T3 is also off. With transistor T3 off, the KF Common line to the Function key switches is clamped to -14 volts via the T3 collector resistor. Only after Key Common goes True enabling the set of KFF2 can transistor T4 turn on. Transistor T4 turning on causes its collector output to be clamped to the emitter voltage VGG and transistor T3 is turned on. With transistor T3 turned on, its collector output is clamped to 0 volts (True) and the signal KF Common will be True. A simplified diagram of the input circuit is shown in Figure 4-33.





Signal diagram on each point of above circuit diagram

INPUT CIRCUITS

FIGURE 4-33

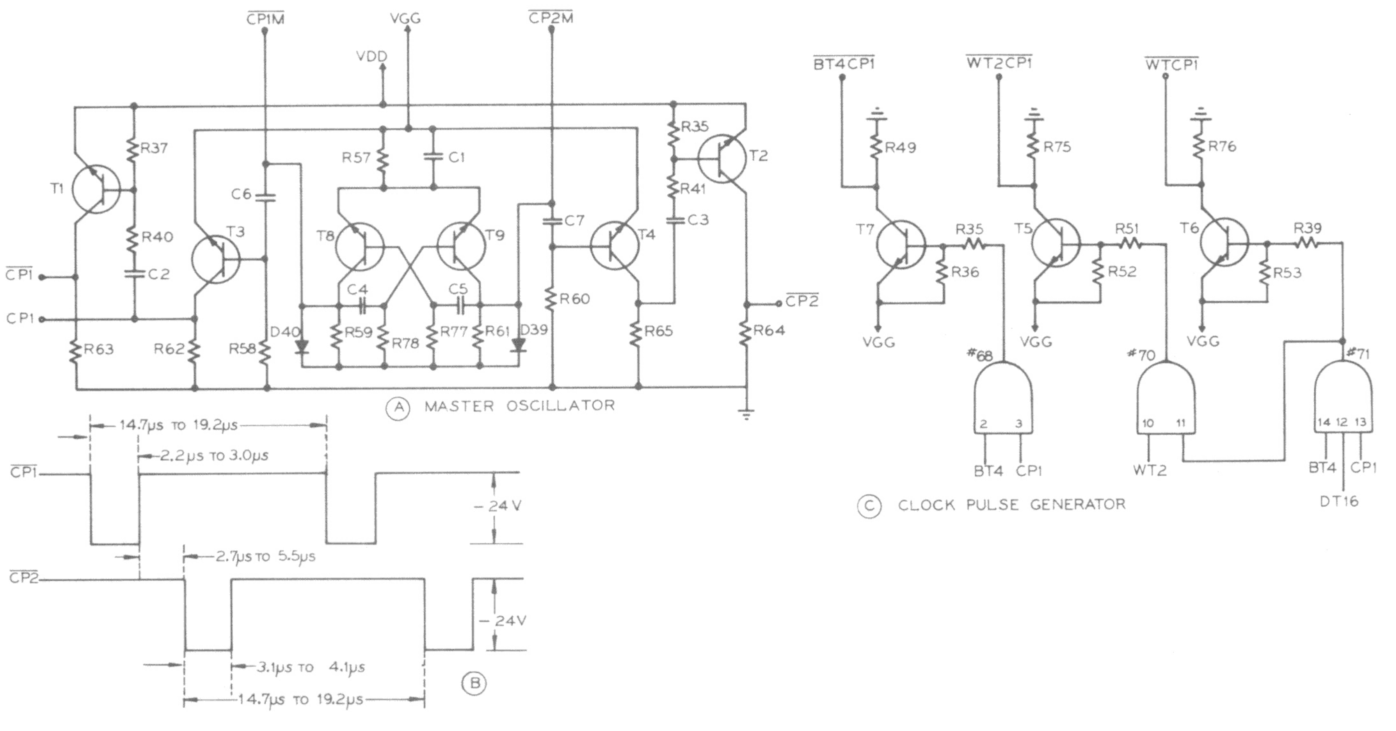
5. MASTER OSCILLATOR AND CLOCK PULSE GENERATOR

The Master Oscillator (Figure 4-34) is composed of an unsymetrical astable multivibrator operating at a frequency of 60KHz ($\pm$8 KHz). A complete operational description of this type of circuit may be found in Lesson 19 of the "Friden Electronics Correspondence Course".

The output waveforms produced at the collectors of transistors T8 and T9 are further shaped by transistors T3 and T4. These outputs are then inverted by transistors T1 and T2 to produce the $\overline{\text{CP1}}$ and $\overline{\text{CP2}}$ clock pulses as shown in Figure 4-34.

Transistors, T5, T6, and T9 are inverter amplifiers used in conjunction with gates 70, 71, and 68 to develop clock pulses $\overline{\text{WT2CP1}}$, $\overline{\text{WTCP1}}$, and $\overline{\text{BT4CP1}}$.

The collector output of transistor T3 is designated CP1 and is used to develop special clock pulses via gates 68, 70, and 71. (Note: The outputs designated CP1M and $\overline{\text{CP2M}}$ are provided for factory production testing only.)



MASTER OSCILLATOR AND CLOCK PULSE GENERATOR

FIGURE 4-34

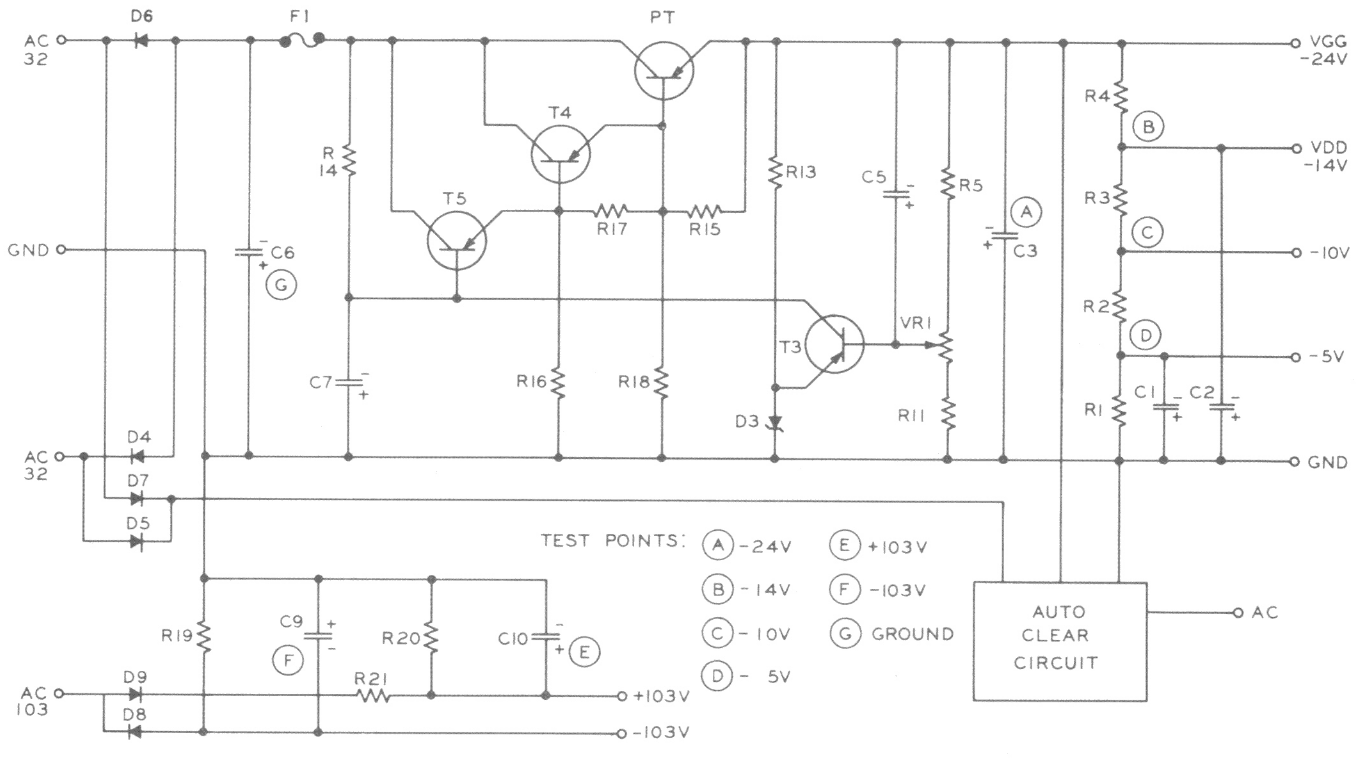
6. POWER SUPPLY

The Power Supply (Figure 4-35) develops a -24V regulated output. The 117 VAC input to the primary of the step down transformer (not shown) is via an 0.05A fuse (F2). The center tapped secondary feeds a full wave rectifier which provides a -32 volt output. Power transistor PT is part of the regulator circuit and approximately 10 volts is dropped across the PT transistor to provide a -24 volt output. A voltage divider tapped off the -24 volt supply provides regulated outputs of -14V, -10V, and -5V.

The voltage regulator circuit utilizes transistors T3, T4, T5, D3 and associated circuitry. Diode D3 provides a 14.5 volt reference for transistor T3. Potentiometer VR1 is used to adjust the -24V regulation by controlling the bias voltage for the regulation sensing transistor T3.

Assuming the -24V output decreases to -23V, the voltage at the base of T3 will go more positive, causing the collector voltage of T3 (Base of T5) to go more negative. T5 being an emitter follower will reflect the negative change at its emitter (Base T4). T4 is also an emitter follower and it reflects the negative change of voltage at the base of the Power Transistor PT causing it to conduct harder and thereby drop less voltage. Therefore, more of the 32 volt rectifier output is available at the output of the power supply and the -24 volt output remains relatively constant. The reverse action will occur if the -24 volt supply attempts to increase toward -25V.

In addition to the -24V regulated supply, a non-regulated -103V and +103V supply is provided via a dual half-wave rectifier circuit. This 103 volt supply is used for operating the Indicator (Nixie) Tubes.



POWER SUPPLY SCHEMATIC

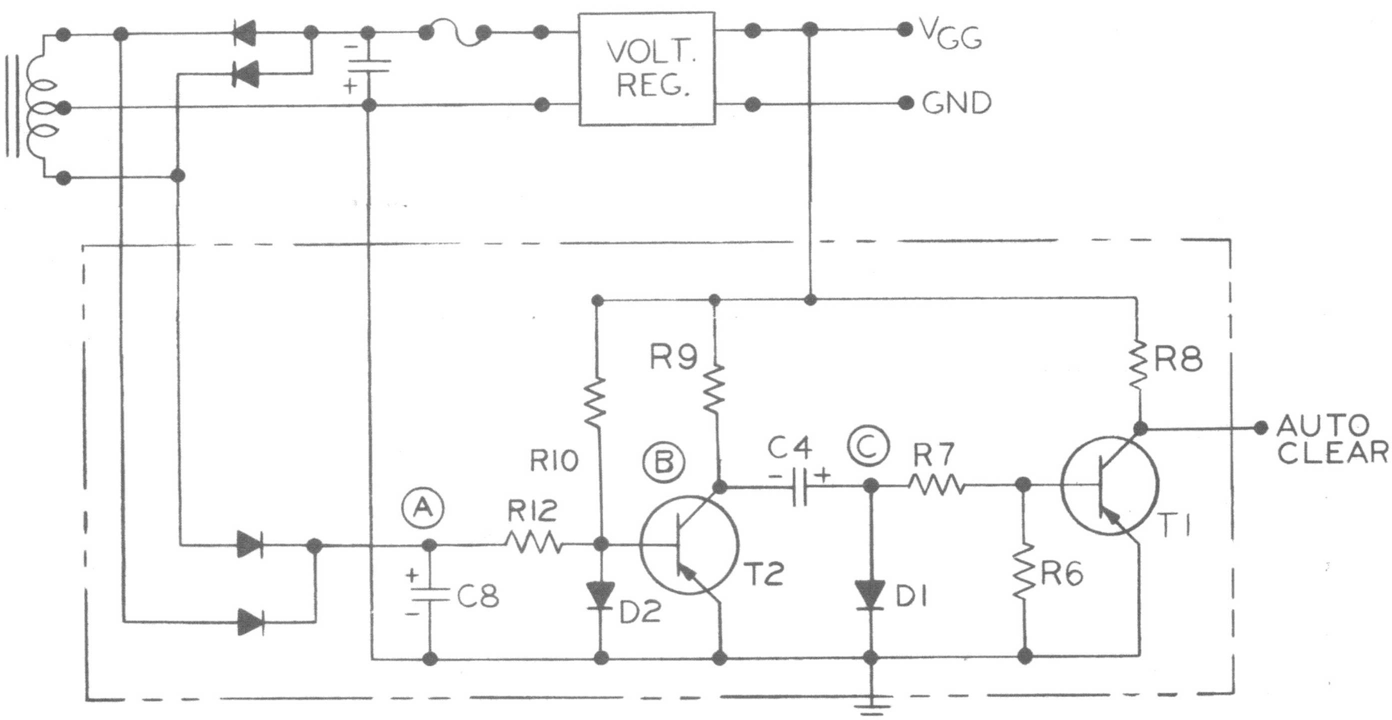
FIGURE 4-35

7. AUTO CLEAR

All registers in the 1115 are cleared automatically via the "Auto Clear" circuit (Figure 4-36) at the time the Power Switch is first turned on.

When the machine is first turned on, Transistor T2 will turn on ensuring that capacitor C4 is discharged to zero volts. Then as capacitor C8 charges, the voltage at point A goes positive, causing T2 to cutoff. With T2 cutoff, capacitor C4 will begin to charge to -24V and its charge current will cause a negative voltage to be felt on the base of T1 allowing T1 to turn on, and its output signal "Auto Clear" to become True (0 volts).

Then, when capacitor C4 becomes fully charged to 24 volts, the voltage at the base of T1 will be approximately zero, causing T1 to turn off and the "Auto Clear" signal to go False for as long as the machine remains on.



AUTO CLEAR

FIGURE 4-36

SECTION 5

MAINTENANCE

SECTION CONTENTS

A. GLOSSARY OF SIGNAL NAMES AND LOGIC EQUATIONS

1. ENTRY SIGNALS

(1) A (Addition): [+–] key signal

(2) S (Subtraction): [–=] key signal

(3) M (Multiplication): [X] key signal

(4) D (Division): [÷] key signal

(5) R (Reverse): [R] key signal

(6) N (Number): Number key signal

(7) P (Point): [.] key signal

(8) BD: Entry data signal of a binary coded decimal number (8-4-2-1 code).

(9) K.(MLT2 + DIV2): [K] key signal

(10) R/OF.K R/O: [R/O] key signal

(11) C + AC: [C] key signal

(12) C + AC + CE: [CE] key signal

2. CONTROL SIGNALS

(1) KFF1 (Key FF 1). This "D" type flip-flop is permissed to be set when the signal Key Common goes true (Logic 1) on depression of a digit or function key. The transition of the flip-flop to the set condition occurs when the clock pulse WT2CP1 occurs.

(2) KFF2 (Key FF 2): This "D" type flip-flop is permissed to be set via logic gate #2 by: Key Common.KFF1. With KFF2 set, the signal KF Common becomes True.

(3) POT (Decimal Point F/F). This flip-flop is set and its output signal POT goes true when the decimal point key is depressed. At the end of the Entry operation, the POT FF is reset by depression of a Function key, or by depression of the Clear or Clear Entry keys.

(4) MLT 1 (Mult 1 F/F). This flip-flop is set and its output signal MLT 1 becomes true when the MULT key is depressed.

(5) DIV 1 (DIV 1 F/F). This flip-flop is set and its output signal DIV 1 becomes true when the DIVIDE key is depressed.

(6) MLT 2 (MULT 2 F/F). This flip-flop is set via the signal MLT1.SOSF and is used as the command signal for a Mult operation.

2. CONTROL SIGNALS (Cont.)

(7) DIV 2 (DIV 2 F/F). This flip-flop is set via the signal DIV1.SOSF and is used as the command signal for a Divide operation.

(8) ENT (ENTRY F/F). This flip-flop is set at the end of a calculation to indicate that the machine is ready to accept another entry. When a Number key, Decimal point, or Reverse key is depressed, the ENT FF is reset.

(9) OSF (Operation Start F/F). This flip-flop is set via the signal SOSF (Set Operation Start FF) which is developed at the output of gates 19 and 21. The Operation Start Signal is used for the Operation Start command.

(10) CDP (Decimal Point Alignment F/F). This flip-flop is set under the various conditions requiring decimal alignment of the contents in the registers with the setting of the Decimal switch.

(11) CHG 1 (Change 1 FF). The output of this flip-flop is used as a command signal to exchange the contents of R2 and R3 for new Entries, Reverse operations, and during Add or Subtract.

(12) AOS (Add or Subtract F/F). When this flip-flop is set, its output signal (AOS) causes the Full Adder and Subtracter (FAS) to perform a calculation of R2±R3N in an Add or Subtract operation; or R1±R3N in a Mult or Divide operation.

(13) CWF (Complement Word F/F). The output of this flip-flop is used to control changing a number to a complement or from a complement. For example, in an Add or Subtract operation, the contents of R2N is fed by way of the "Y" input into FAS for one word time after the answer has been developed. If the result of the subtraction is a complement number in R2N, the contents of R2N are subtracted from "0" which results in changing the complement number to a positive number.

(14) OVF1 (Overflow 1 F/F). This flip-flop is used for detecting a complement number during a subtract operation.

(15) R/OF (Round Off F/F). This flip-flop is set during the last step of each calculation and the signal is used to perform a round off function on the LSD of the digit in R2N-1.

(16) FAS Sub (OR Gate). During the time this signal is True at pin #18 on the FAS IC chip, FAS will act as a subtracter.

(17) FAS Sub1 (FAS Subtraction F/F). This flip-flop sets to indicate a machine subtract is to be accomplished.

(18) RIGHT SHIFT (RSH F/F). The output signal from this flip-flop enables a right shift of the contents of R1 and R2N.

(19) LEFT SHIFT (LSH F/F). The output signal from this flip-flop enables a left shift of the contents of R1 and R2N.

2. CONTROL SIGNALS (Cont.)

(20) MULT AND DIVIDE (MDF F/F). The output signal from this flip-flop enables the repeat operations necessary in mult or divide. The MDF FF is always set simultaneously with the OSF FF via the signal SOSF.

(21) INDICATOR REGISTER SIGN (IRS F/F). The contents of R2S are shifted out of R2 during DT2 time and if the sign of the number being displayed is negative, the signal R2.DT2 at gate #43 will be True. Then, at $\overline{\text{BT4CP1}}$ time, the IRS FF is permissed to set and its output going True enables the Transistor T36 to turn on and the "Minus" Indicator light will turn on.

(22) FF1 (F/F #1). When the contents of R2P are different from the setting of the Decimal Switch, the FF1 FF is set and its output signal FF1 being True enables an alignment operation.

(23) FF2 (F/F #2). This flip-flop is used in conjunction with FF1 to enable a shift operation (alignment). The signal FF2 enables a right shift. The signal $\overline{\text{FF2}}$ enables a left shift.

(24) R2F (R2 F/F). This flip-flop is used as a control for various operations of Mult and Divide functions.

(25) OVERFLOW 2 (OVF2 F/F). When the machine is in an Overflow condition, the OVF2 FF is set and the drive circuit (Transistor T1) is enabled, causing the Overflow Light to turn on.

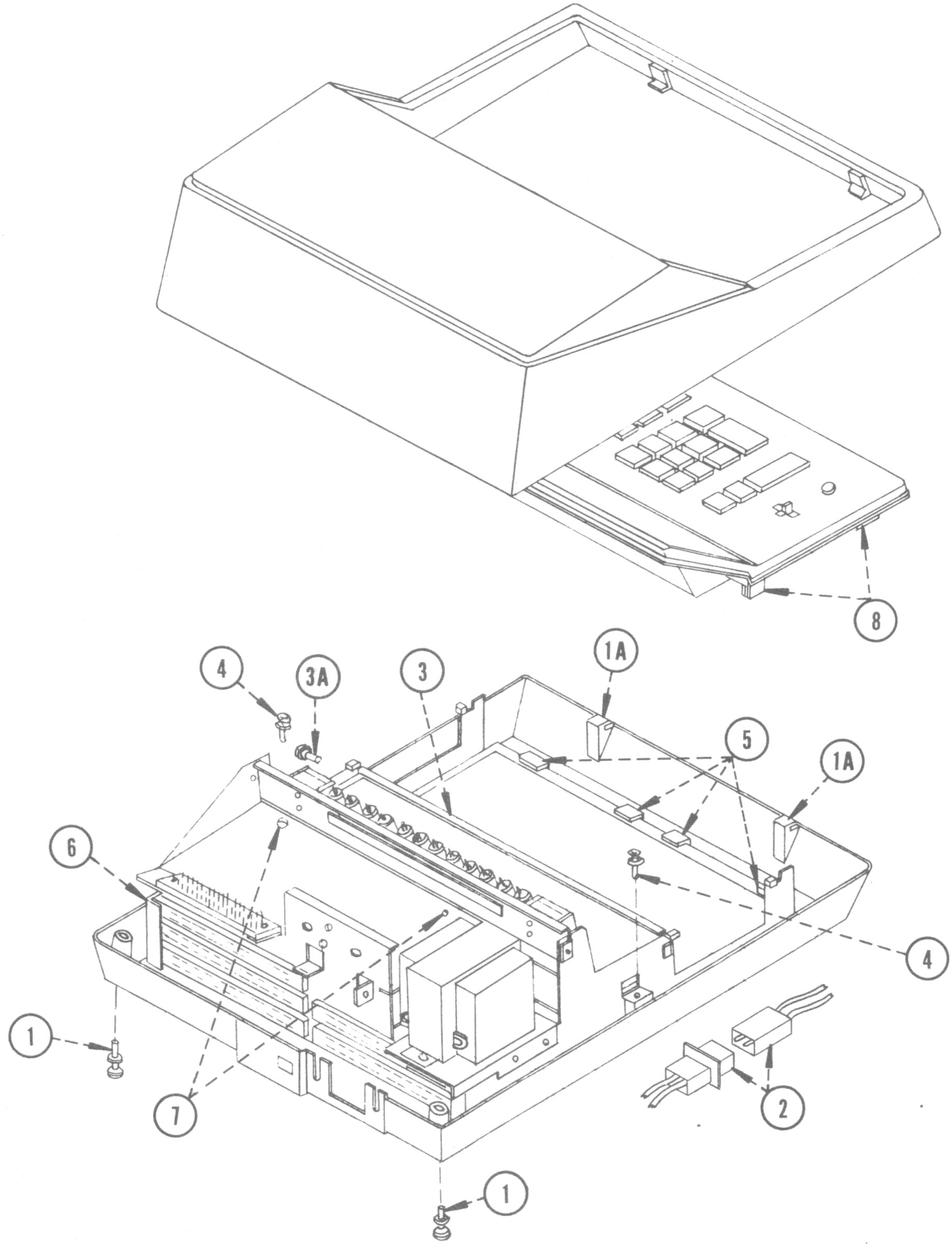


FIGURE 5-1

B. DISASSEMBLY AND ASSEMBLY

Instructions for disassembly and assembly of the component parts of the 1115 are listed below. Each instruction is keyed to Figure 5-1.

(1) To remove the top cover, remove 2 screws (item 1) from the bottom of the machine (rear) and lift the cover from the rear so it disengages the locking tabs from the slots in the front panel (1A).

(2) To remove the keyboard from the chassis, disconnect the plug (item 2) and lift the keyboard off the chassis side frames. To remove the keyboard from the machine, disconnect the keyboard ground wire, and uncouple the connector plug at the right rear of the PC card holder.

(3) To remove the PC cards:

(a) Remove card holder plate (item 3) by removing screw 3A.

(b) Remove two screws (item 4) securing the PC card holder frame to the base.

(c) Lift the rear of the chassis and move it rearward to disengage the chassis retainer tabs and the #31 PC card from the retainer slots (item 5).

(d) PC cards #31, #32, and #33 can now be removed by prying them forward with a screwdriver inserted in the appropriate holes in the side frame (6).

(e) PC card #34 is removed by removing the two screws (7) and lifting the card up.

(4) To reassemble the components, reverse the order of disassembly listed above. Also the following precautions should be observed.

(a) When the chassis containing the PC cards is being reinstalled, be sure that the retainer tabs on the front edge of the chassis, and the #1 PC card are engaged in their respective retainer slots (5).

(b) When reinstalling the keyboard assembly:

(1) Be sure that the slotted tabs and locator grooves in the keyboard assembly (item 8) are engaged with their corresponding points on the chassis side frames.

(2) Check to see that the keyboard grounding strap is making good contact with the Card Holder Plate.

(c) Before installing the top cover, make sure that the wires and cables are out of the way so they don't get pinched when the cover is secured.

C. INSPECTION PROCEDURE

(1) Perform a complete operational check using the test problems starting on page 5-6. NOTE: Check to see that all numbers in the indicating tubes are operating properly.

(2) Visually inspect the machine for worn or loose parts such as keystems, keytops, On/Off switch, Decimal Switch, etc. (Replace parts if necessary.)

(3) Check the -24V output of Test Point "A" (negative side of capacitor C3) on PC card #34 to see that it is within the tolerance of -22.8V to -25.2V. (See Adjustment #2, Power Supply, page, 5-4 for location and adjustment procedure.) NOTE: Connect a ground wire from the positive side of capacitor C6 (Test Point G) to the card holder side frame before making the voltage measurement.

(4) Clean and Lubricate keyboard unit as necessary.

(a) Blow out all dust and foreign material.

(b) Lightly lubricate the top and bottom of the keystems using a small amount of grease (Shell non-stain 71212/Friden MS-136) applied with the tip of a long long bladed screwdriver. Use care to prevent grease from getting on the #31 PC card because grease will damage the protective coating on the card.

(5) Check the adjustment of all reed switches on the keyboard.

(a) Each reed switch should close when its keystem has been depressed approximately half way down. See Reed Switch adjustments, page 5-10, for adjustment procedure.

(6) Clean the exterior of the machine with soap and water. Avoid any commercial cleaner that is not recommended for use with plastic.

D. OPERATIONAL CHECK

The procedures for accomplishing a complete operational check of the 1115 are listed below. The entire sequence should be followed after replacing a PC board or after completion of a repair.

1. Check of decimal set switch, round off, and truncate operation. FP = preset position of decimal switch. R/O ↑ = Round off switch up. R/O ↓ = Round off switch latched down.

				(Operation)		(Indication)	
(a)	FP=5	R/O	↑	1.23456789	−=	. . . . . 1.23456	C
(b)	FP=5	R/O	↓	123	+=	. . . . 123.00000	C
(c)	FP=2	R/O	↓	1.23567890	+=	. . . . . . 1.24	C
(d)	FP=0	R/O	↓	1.56789000	+=	. . . . 2.	C
(e)	FP=0	R/O	↑	1.56789000	+=	. . . . 1.	C

D. OPERATIONAL CHECK (Cont.)

2. Check of addition and subtraction

FP=5 and [R/O] ↓

(a) 123.123 [+=] 0.123123 [+=] 1231231.23 [+=]
1231231.23123 [+=] 2462585.70735

(b) C 0.00123 [−=] 1.23 [−=] 1230 [−=]
1231.23123 [−=] 2462.46246 [−=] 1.23 [+=]
1.23 [+=] 1.23 [+=] 1.23 [+=] . . . . . . 4920.00492- (NEG)

3. Check of multiplication and division

At FP=5 and [R/O] ↓

(a) 1234.5679 [X] 7.2 [+=] 8888.88888

(b) 12345679 [X] 0.36 [+=] 4444444.44000

(c) 1.23000000000 [X] 1.23000000000 [+=] . . . 1.51290

(d) 1111.11 [X] [+=] 1234565.43210

(e) 15129 [÷] 12300000 [+=] 0.00123

(f) 45600 [÷] 0.01 [−=] 4560000.00000-

(g) 123 [X] [+=] [X] 12.3 [X] 1.23 [X] 1.23 [÷] 123 [÷]
1.23 [÷] 1.23 [+=] 1512.90000

4. Check of constant calculation

FP-5, [R/O] ↓ [K] ↓

(a) 123 [X] [+=] 15129.00000
[+=] 1860867.00000

D. OPERATIONAL CHECK (Cont.)

2	[+=]	246.00000
3	[+=]	369.00000
	[+=]	45387.00000
	[+=]	5582601.00000
÷ 123	[+=]	45387.00000
	[+=]	369.00000
	[+=]	3.00000
2	[+=]	0.01626
3	[+=]	0.02439

5. Check of reverse calculation

FP=5 [R/O] ↓

123 [−=] 456 [R] [+=] [X] [R] [+=] [÷] [R] [+=] 333.00000

6. Overflow check

Confirm the overflow light after each of the following calculations.

FP=2 [R/O] ↓

(a) 1234567890123 . . . . overflow light comes on

(b) 9999999999 [+=] 1 [+=] . . " " "

(c) 9999999999 [−=] 1 [−=] . . " " "

(d) 9999999999.99 [+=] 0.006 [+=] " " "

(e) 999999 [X] [+=] . . . " " "

(f) 1000000000 [÷] 0.1 [+=] " " "

E. TROUBLESHOOTING

Prior to attempting to repair or service the 1115 Electronic Calculator, be sufficiently well informed concerning the operating conditions in the customer's office such as: Excessive high or low temperature (operating temperature 32° F. to 104°F.); proper line voltage (115 volts ±10%, 50/60 Hz.); excessively high humidity; and that correct operating procedures are being observed.

Locate and repair obvious problems such as: blown fuses, sticking keys, etc. Any complicated condition which requires a relatively long service time should be accomplished by exchanging subassemblies such as logic cards and keyboard. These can then be returned to the branch office for repair, or sent to the Service Center in your area for repair.

1. PC BOARD REPLACEMENT

If the PC boards are suspected of causing trouble, special precautions must be observed while replacing or troubleshooting the boards due to the extreme sensitivity of the MOS IC circuits. Replace only one board at a time while observing the following precautions.

(1) Turn the Power Switch "OFF" before replacing a PC board. If a board is removed or installed with the power on, possible damage to the components such as IC's, transistors and diodes may occur.

(2) Avoid indiscriminate touching of the IC's with your bare fingers. Due to their electrical characteristics, the MOS IC's used in the 1115 have an extremely high input impedance and are very sensitive to static charges (especially when the PC boards are removed from the machine). Handle the boards only by the metal side frames.

(3) When the PC boards are not in use or while transporting or shipping individual boards, be sure to short circuit the terminals with a protective connector. (Two each, Part #KCA 22035 with all pins soldered together.) Protective connectors with short circuited pins are used to maintain all PC board contacts at an equal potential so that no potential difference exists between the IC leads. However, not all the IC leads are connected to the PC contacts and care must be taken to prevent touching the IC leads with the fingers.

(4) Avoid damaging the components mounted on the PC boards. Damage to the components can occur or their insulation may be lowered if the PC boards are allowed to contact each other, or are stacked one on top of the other.

(5) Avoid external force or shock to the PC boards.

(6) Do not insert a PC board into a connector for another board. Also, since the connecting terminals of the PC boards are arranged symmetrically, it is possible to insert a board upside down. Therefore, check to see that the component side of the board is facing up, prior to inserting it. The proper arrangement of the PC boards in the machine is #31 through #34 with the #31 board at the bottom

(7) Before connecting any test leads, or using a soldering iron, the logic ground must be connected to the chassis ground. This can be done by connecting a test clip lead wire between the positive (+) side of C6 (470 mfd electrolytic capacitor on card #34 Test point G) and chassis ground or "Scope" ground.

(8) Perform the operational check after each replacement of a PC board.

The basic card functions are listed to help diagnose troubles.

Card #31 Entry and Control Functions (Master & Conditional Control)
Card #32 Master Oscillator and Shift Registers
Card #33 Display Decoding, Number Indicating Tubes, and Digit Counter
Card #34 Power Supply

NOTE: Card extender, tool #18770, designed for use on the 1150 Printing Calculator can be modified for use on the 1115 Calculator by removing the card extractor on each side of the card. When using the modified extender on an 1115 PC card, be sure to insulate the exposed terminals with electrical tape or equivalent insulating material.

2. REPLACEMENT OF COMPONENTS ON PC BOARDS

(1) When replacing broken or burned resistors, it may be necessary to use insulating tubing on the leads of the stand up type resistors to prevent shorting with adjacent resistors.

(2) When replacing IC's, be sure to align the locator on the IC with the locator on the PC card as shown in Figure 5-5.

F. ADJUSTMENTS

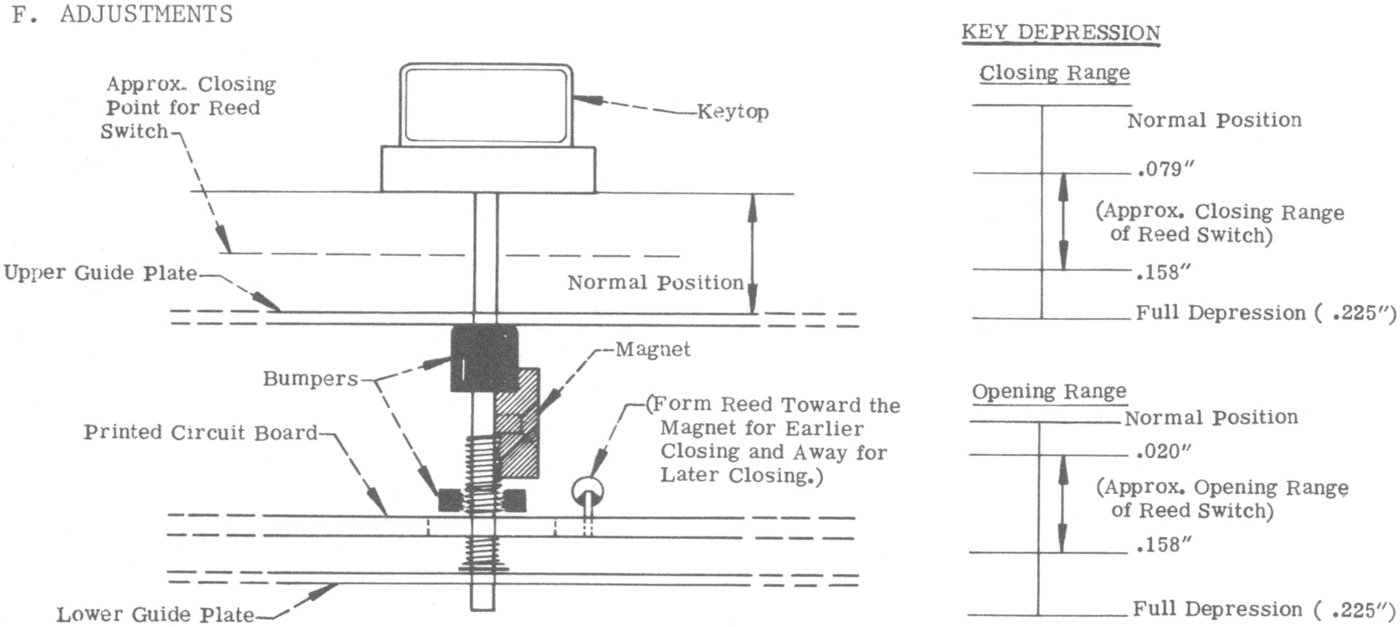


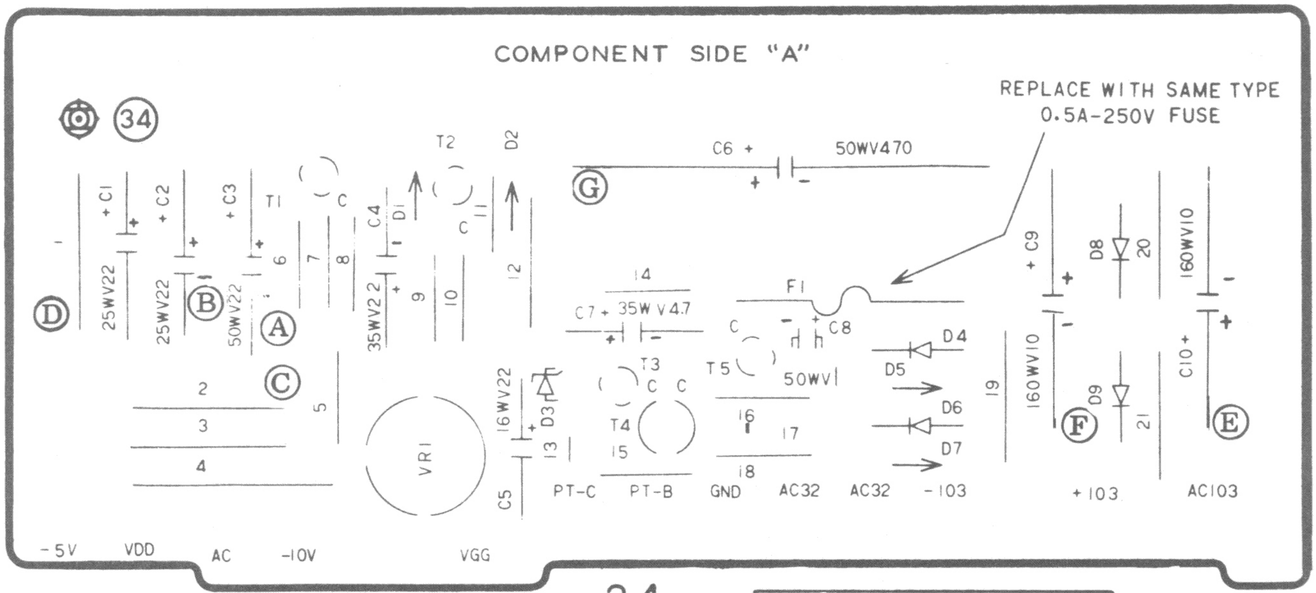
FIGURE 5-2

1. KEYBOARD

The keyboard reed switches must close when their respective keystems have been depressed approximately half way down. To adjust, move the individual reed switches closer or farther away from their respective magnets as shown in Figure 5-2.

(NOTE: Moving the switches closer to the magnets causes them to close sooner. Moving them farther away from the magnets causes them to close later.)

F. ADJUSTMENTS (Cont.)



34

TEST POINTS		
A=-24V	D=-5V	G=0V
B=-14V	E=+103V	
C=-10V	F=-103V	

FIGURE 5-3

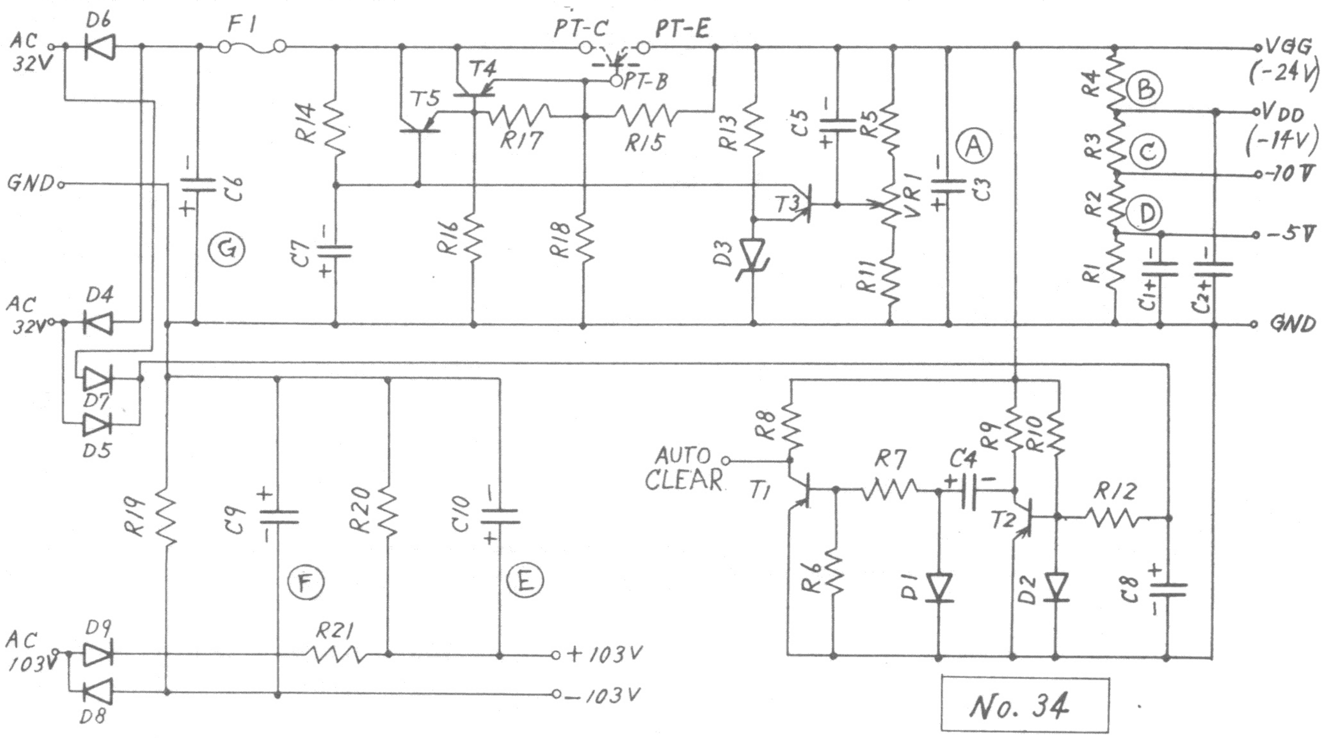
2. POWER SUPPLY

The -24V output at Test Point "A" (negative side of C3) on PC card #34 should read -24V or within the tolerance of -22.8V to -25.2V. The adjustment is made by turning the shaft on potentiometer VR1 as required. After making the adjustment, the shaft should be secured with Locktite, or other suitable cement.

(NOTE: Prior to checking any voltages, connect a ground wire from the positive side of capacitor C6 (Test Point G) to the card holder side frame.)

Test Points B, C, D, E, and F should also be checked and their outputs should be within the specified tolerance range: Point B, -14V (-13.5V to -15.3V); Point C, -10V (-8.5V to -11.5V); Point D, -5V (-3V to -6.3V); Point E, +103V (+75V to +100V); Point F, =103V (-90V to -115V); Point G, 0V.

2. POWER SUPPLY (Cont.)



POWER SUPPLY SCHEMATIC

FIGURE 5-4

a. SCHEMATIC. For convenience of the CSRep, a schematic of the Power Supply is shown in Figure 5-4 with the voltage test points indicated.

G. COMPONENT IDENTIFICATION AND LAYOUT

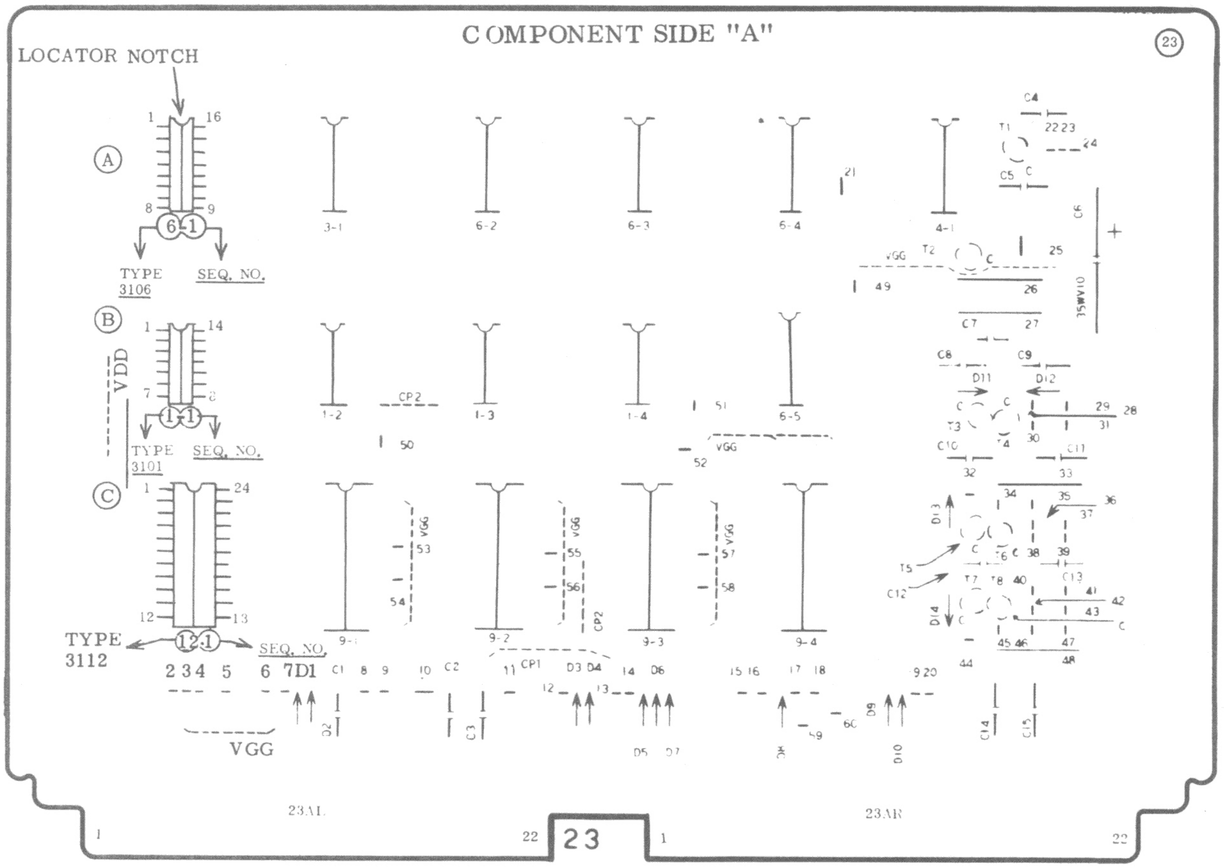


FIGURE 5-5 COMPONENT IDENTIFICATION*

1. PRINTED CIRCUIT BOARD

For identifying and locating components or terminal pins on the printed circuit boards, the board should be viewed as shown in Figure 5-5. Each component is identified and numbered on the board from left to right starting at the top, left hand side of the board. *NOTE: The PC board shown in Figure 5-5 is not used in the 1115 machine but is used in the illustration since it is typical of the PC boards used in this series of Electronic Calculators.

Resistors:	Indicated on PC board as 1, 2, 3, etc. and numbered from left to right.
Diodes:	Indicated on PC board as D1, D2, D3, etc. and numbered from left to right.
Capacitors:	Indicated on PC board as C1, C2, C3, etc. and numbered from left to right.
IC Chips:	Indicated symbolically by a centerline drawn between the two ends and with the notched end at the top. The two numbers at the end of the chip are interpreted as follows: The 1st number indicates the last digit of the IC type. For example, IC 3106 would be indicated by a "6". The 2nd number indicates the successive use of that particular type of chip on the PC board. For example, 6-1 indicates a type 3106 IC chip, and "1" indicates its sequence number. The system is illustrated in "A", "B", and "C" of Figure 5-5. Also shown in Figure 5-5 is the pin numbering arrangement used on the 3 sizes of IC chips used in the 1115.

2. NUMBER INDICATING TUBES

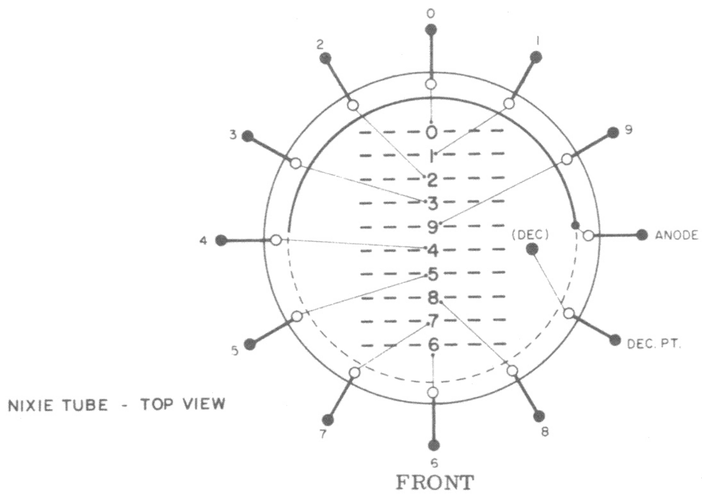


FIGURE 5-6

Shown in Figure 5-6 is a top view of a number indicating tube which illustrates the relative position of the number cathodes, the decimal point, and the anode inside the tube. Also shown are the internal and external connections to the cathodes and the anode.

3. TRANSISTORS

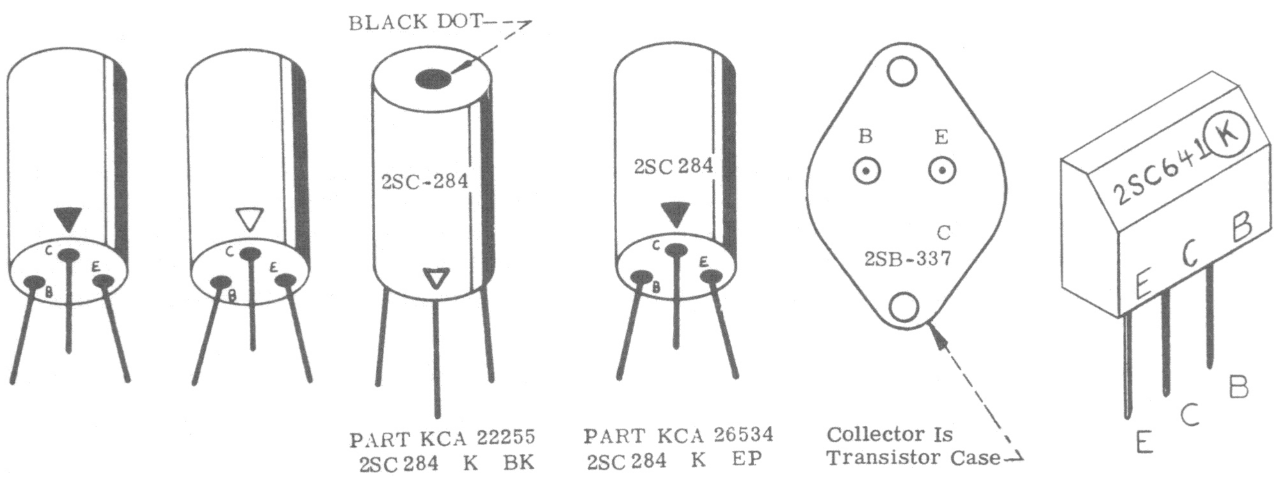


FIGURE 5-7

In Figure 5-7, are shown the various transistors used in the 1115 machine and their Collector, Emitter, and Base lead identification. To distinguish the difference between the two transistors having the same type number 2SC284, one has a black dot on its top. The Part Numbers and type identification for these two transistors are as indicated in the illustration.

4. DIODES

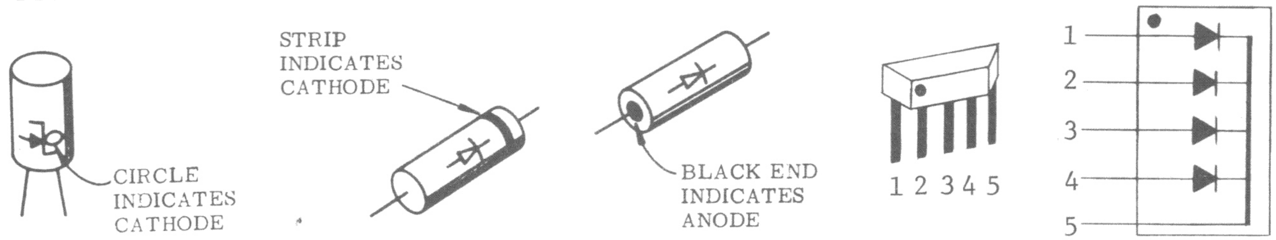
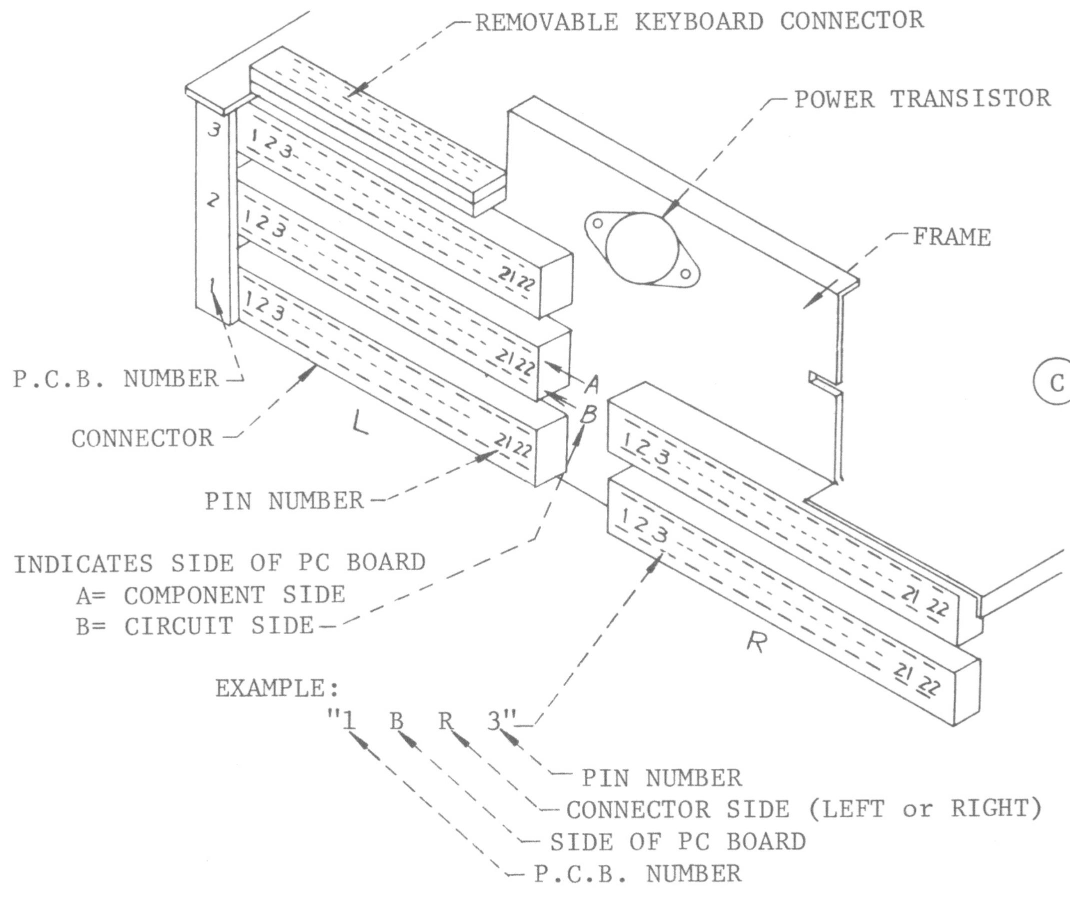
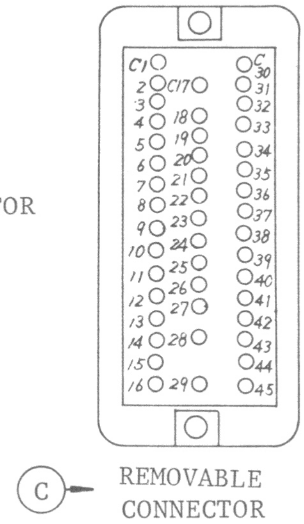


FIGURE 5-8

As shown in Figure 5-8, a small circle is used to indicate the cathode lead on the zener diode, a stripe is used to indicate the cathode on the diodes, or a black dot on the end of a diode indicates its anode lead. The diode array is a module containing four diodes with a common cathode. The terminals are identified as indicated in the drawing. NOTE: Dot on module indicates #1 lead.

5. PC BOARD CONNECTOR ASSEMBLY





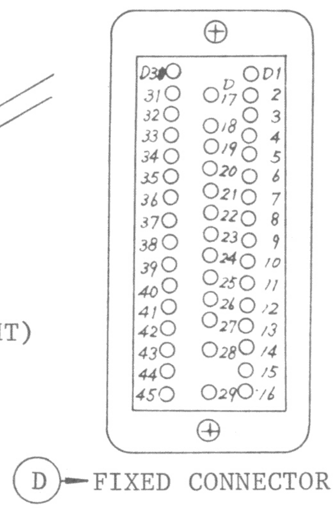


FIGURE 5-9

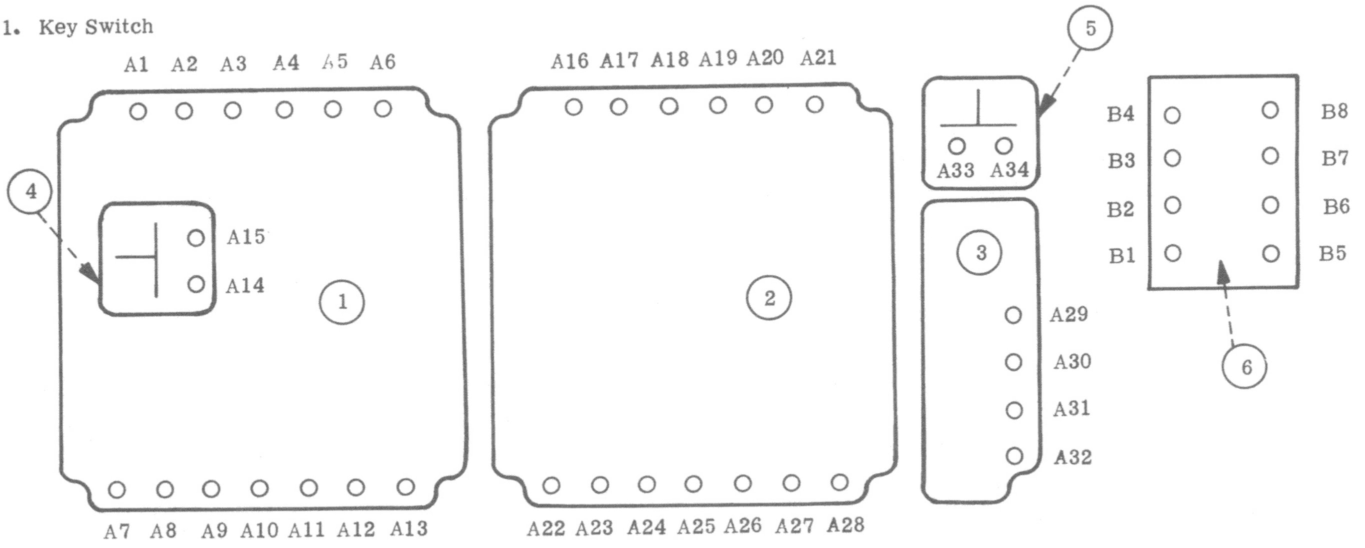
In Figure 5-9 is the PC Board Connector Assembly. The various identification points associated with the PC boards that are inserted in the plug connectors are as shown.

6. EXTERNAL TERMINAL NUMBER IDENTIFICATION

In Figure 5-10 are shown the connector terminals for the Keyboard, Decimal Set Switch, Power Transistor, Transformer, and Indicating Lights.

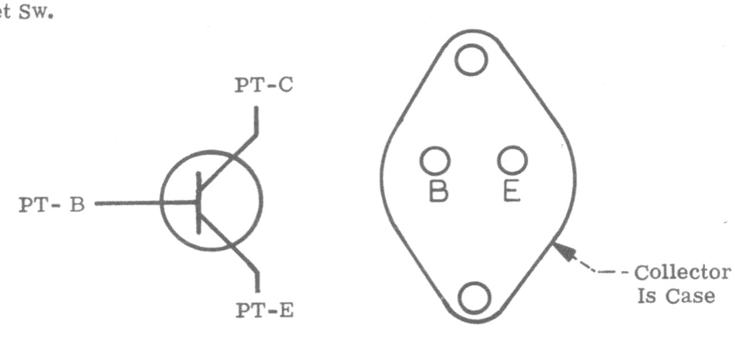
TERMINAL NUMBER

1. Key Switch

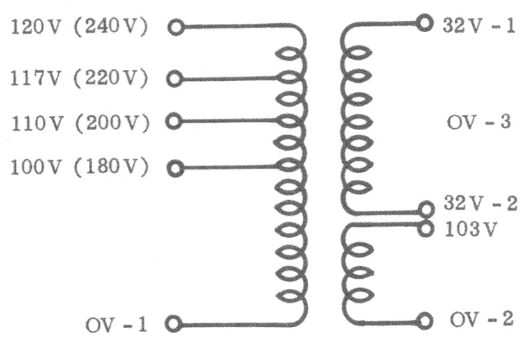


1. Function Key Set
2. Number Key Set
3. Clear Key Set
4. [R/0] Key (Latch Down Type)
5. [K] Key (Latch Down Type)
6. Decimal Set Sw.

3. Power Transistor (Type : 2SB337)



4. Transformer



5. Indicating Light (Neon Tube)

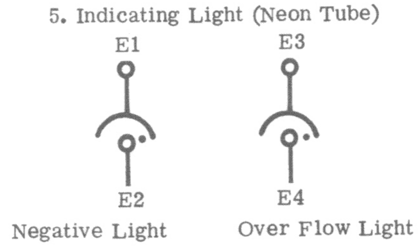
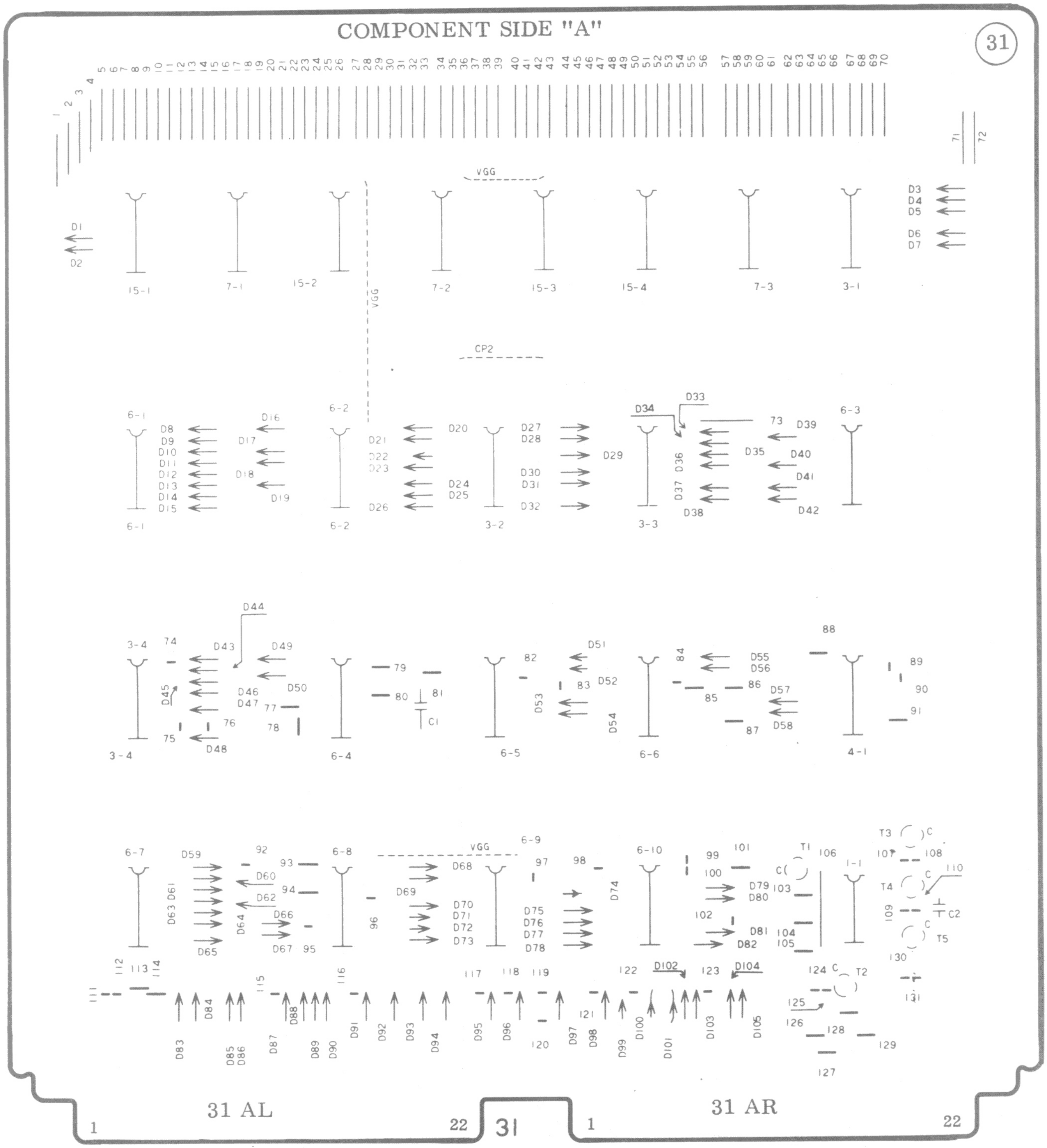


FIGURE 5-10

H. PRINTED CIRCUIT CARDS AND COMPONENT LISTS



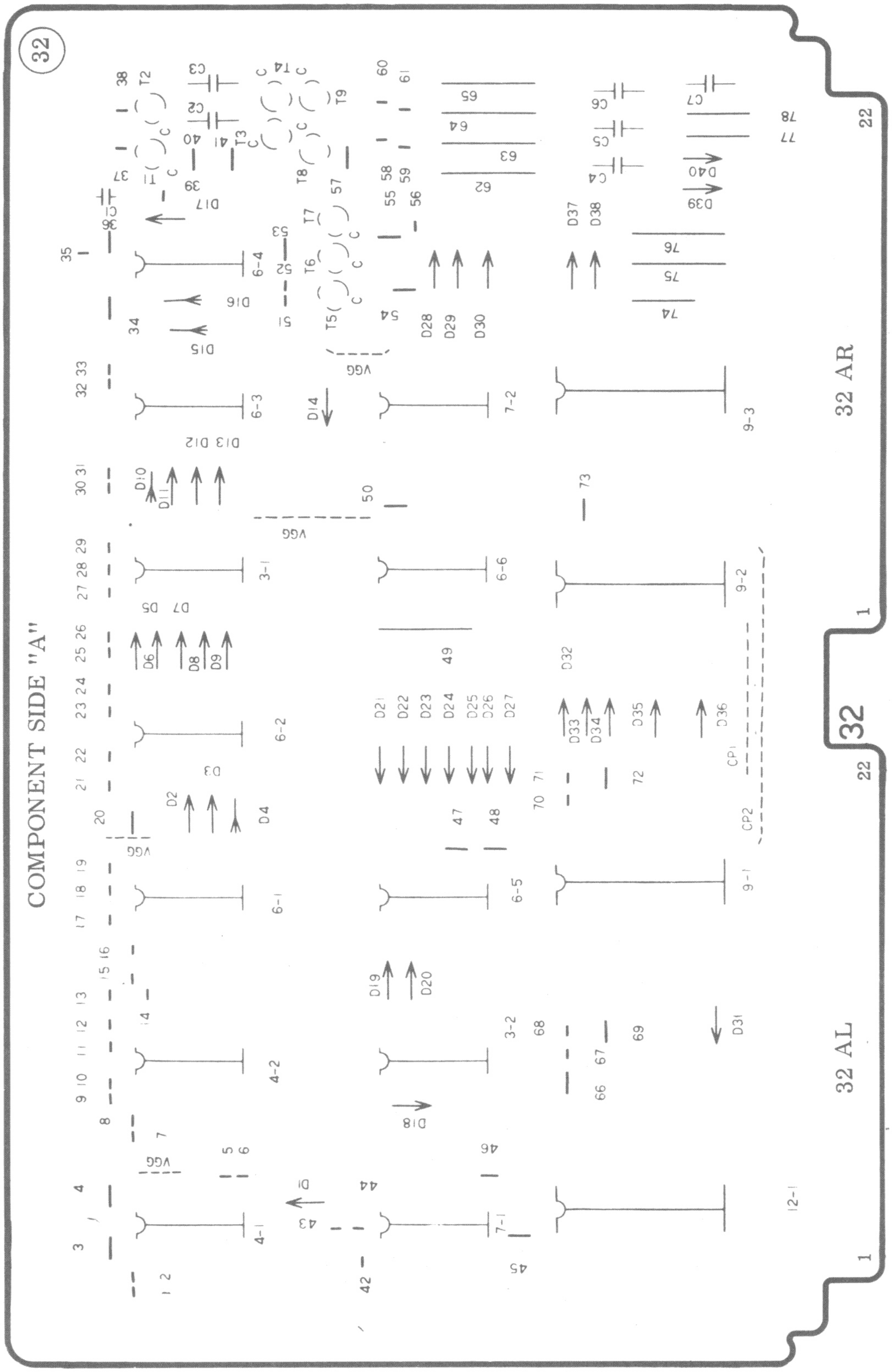
LOGIC CARD #31 (Entry and Control Function Logic)

COMPONENT LIST FOR PC CARD #31

P.C.B NO. 31

MOS IC		8	1/8 330kΩ	42	1/8 220kΩ	76	Ⓥ 1/8 220kΩ	110	Ⓥ 1/8 56kΩ	9	1S2075	43	1S2075	~~77~~	~~1S2075~~ ※	T	TRANSISTOR
1-1	HD3101	9	" "	43	" 100kΩ	77	" " 100kΩ	111	" " 100kΩ	10	"	44	"	~~78~~	~~" "~~ ※	1	2SC284Ⓚ EP
3-1	HD3103	10	" 220kΩ	44	" 220kΩ	78	" " "	112	" " "	11	"	45	"	79	1S2075	2	"
2	"	11	" "	45	" "	79	" " "	113	" " "	12	"	46	"	80	"	3	2SA617Ⓚ
3	"	12	" 330kΩ	46	" 100kΩ	80	" " "	114	" " "	13	"	47	"	81	"	4	2SC284Ⓚ EP
4	"	13	" 220kΩ	47	" "	81	" 1/4 2.2MΩ	115	" " 330kΩ	14	"	48	"	82	"	5	2SA617Ⓚ
4-2	HD3104	14	" 100kΩ	48	" "	82	" 1/8 330kΩ	116	" " "	15	"	49	"	83	"		
6-1	HD3106	15	" "	49	" "	83	" " "	117	" " "	16	"	50	"	84	"		
2	"	16	" "	50	" "	84	" " 100kΩ	118	" " "	17	"	51	"	85	"		
3	"	17	" 220kΩ	51	" "	85	" " "	119	" " "	18	"	52	"	86	"		
4	"	18	" 100kΩ	52	" 56kΩ	86	" " "	120	" " "	19	"	53	"	87	"		
5	"	19	" 220kΩ	53	" 100kΩ	87	" " "	121	" " "	20	"	54	"	88	"		
6	"	20	" 100kΩ	54	" 56kΩ	88	" " "	122	" " "	21	"	55	"	89	"	C	CAPACITOR
7	"	21	" 220kΩ	55	" "	89	" " 330kΩ	123	" " "	22	"	56	"	90	"	1	50WV 1000PF
8	"	22	" 100kΩ	56	" "	90	" " 100kΩ	124	" " 33kΩ	23	"	57	"	91	"	2	50WV 0.1 μF
9	"	23	" "	57	" 220kΩ	91	" " 220kΩ	125	" " 33kΩ	24	"	58	"	92	"		
10	"	24	" "	58	" 100kΩ	92	" " 100kΩ	126	" " 22kΩ	25	"	59	"	93	"		
7-1	HD3107	25	" "	59	" 220kΩ	93	" " "	127	" " 330kΩ	26	"	60	"	94	"		
2	"	26	" "	60	" 100kΩ	94	" " "	128	" " 10kΩ	27	"	61	"	95	"		
3	"	27	" 330kΩ	~~61~~	~~" "~~	95	" " "	129	" " "	28	"	62	"	96	"		
15-1	HD3115	28	" "	62	1/8 100kΩ	96	" " "	130	" " "	29	"	63	"	97	"		
2	"	29	" "	63	" "	97	" " 330kΩ	131	" " 1.2kΩ	30	"	64	"	98	"		
3	"	30	" "	64	" 330kΩ	98	" " 100kΩ			31	"	65	"	99	"		
4	"	31	" 220kΩ	65	" 100kΩ	99	" " "			32	"	66	"	100	"		
		32	" 100kΩ	66	" 220kΩ	100	" " "			33	"	~~67~~	~~" "~~ ※	101	"		
		33	" 330kΩ	67	" 100kΩ	101	" " "	D	DIODE	~~34~~	~~"~~	68	1S2075	102	"		
R	RESISTOR	34	" 100kΩ	68	" 220kΩ	102	" " "	1	1S2075	35	1S2075	69	"	103	"		
1	1/8 220kΩ	35	" 330kΩ	69	" "	103	" " 3.3kΩ	2	"	36	"	70	"	104	"		
2	" 100kΩ	36	" 100kΩ	70	" 330kΩ	104	" " 22kΩ	3	"	37	"	~~71~~	~~" "~~ ※	105	"		
3	" "	37	" "	71	" "	105	" " 100kΩ	~~4~~	~~"~~	38	"	~~72~~	~~" "~~ ※				
4	" "	38	" "	72	" "	106	1/4 5.6kΩ	5	1S2075	39	"	73	1S2075				
5	" "	39	" "	73	" 220kΩ	107	Ⓥ 1/8 1.2kΩ	6	"	40	"	74	"				
6	" "	40	" "	74	Ⓥ 1/8 100kΩ	108	" " 10kΩ	7	"	41	"	75	"				
7	" "	41	" "	75	" " "	109	" " "	8	"	42	"	76	"				

LOGIC CARD #32 (Master Oscillator and Shift Registers)

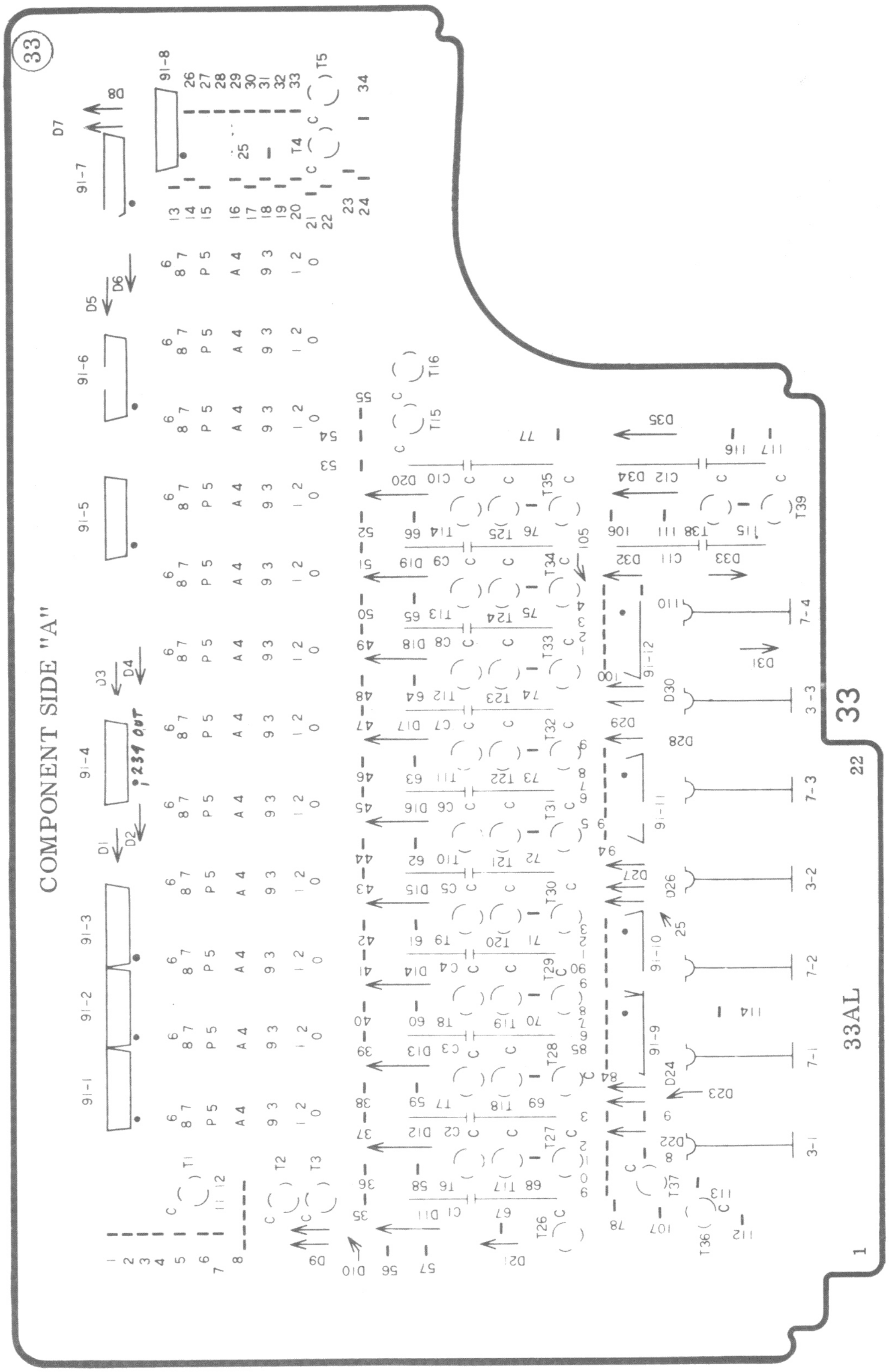


COMPONENT LIST FOR PC CARD #32

P.C.B NO. 32

MOS IC		13	Ⓤ 1/8 12kΩ	47	Ⓤ 1/8 100kΩ			29	1S2075	T	TRANSISTOR
3-1	HD3103	14	" " 100kΩ	48	" " "			30	"	1	2SC284Ⓡ EP
2	"	15	" " 33kΩ	49	1/4 5.6kΩ			31	"	2	"
4-1	HD3104	16	" " 100kΩ	50	Ⓤ 1/8 56kΩ			32	"	3	"
2	"	17	" " 56kΩ	51	" " 22kΩ			33	"	4	"
6-1	HD3106	18	" " 100kΩ	52	" " 4.7kΩ	D	DIODE	34	"	5	"
2	"	19	" " 56kΩ	53	" " 3.3kΩ	1	1S2075	35	"	6	"
3	"	20	" " 100kΩ	54	" " 100kΩ	2	"	36	"	7	"
4	"	21	" " "	55	" " "	3	"	37	"	8	"
5	"	22	" " "	56	" " "	4	"	38	"	9	"
6	"	23	" " "	57	" " 1.8kΩ	5	"	39	"		
7-1	HD3107	24	" " "	58	" " 33kΩ	6	"	40	"		
2	"	25	" " "	59	" " 1.2kΩ	7	"				
9-1	HD3109	26	" " "	60	" " 47kΩ	8	"				
2	"	27	" " 56kΩ	61	" " 1.2kΩ	9	"				
3	"	28	" " 100kΩ	62	1/4 1.2kΩ	10	"				
12-1	HD3112	29	" " "	63	" 3.9kΩ	11	"				
		30	" " "	64	" 3.3kΩ	12	"				
		31	" " "	65	" 1.2kΩ	13	"	C	CAPACITOR		
		32	" " "	66	Ⓤ 1/8 100kΩ	14	"	1	50WV 0.1µF		
		33	" " "	67	" " "	15	"	2	" 680PF		
R	RESISTOR	34	" " "	68	" " "	16	"	3	" 470PF		
1	Ⓤ 1/8 12kΩ	35	" " 22kΩ	69	" " "	17	"	4	" 220PF		
2	" " "	36	" " 3.3kΩ	70	" " "	18	"	5	" "		
3	" " 39kΩ	37	" " "	71	" " 56kΩ	19	"	6	" "		
4	" " 100kΩ	38	" " "	72	" " 100kΩ	20	"	7	" "		
5	" " 12kΩ	39	" " 22kΩ	73	" " "	21	"				
6	" " "	40	" " 10kΩ	74	1/8 100kΩ	22	"				
7	" " "	41	" " 8.2kΩ	75	1/4 5.6kΩ	23	"				
8	" " "	42	" " 100kΩ	76	" "	24	"				
9	" " 56kΩ	43	" " 56kΩ	77	1/8 56kΩ	25	"				
10	" " 12kΩ	44	" " 100kΩ	78	" 39kΩ	26	"				
11	" " 330kΩ	45	" " "			27	"				
12	" " 100kΩ	46	" " "			28	"				

LOGIC CARD #33 (Display Decoding, Number Indicating Tubes & Digit Counter)

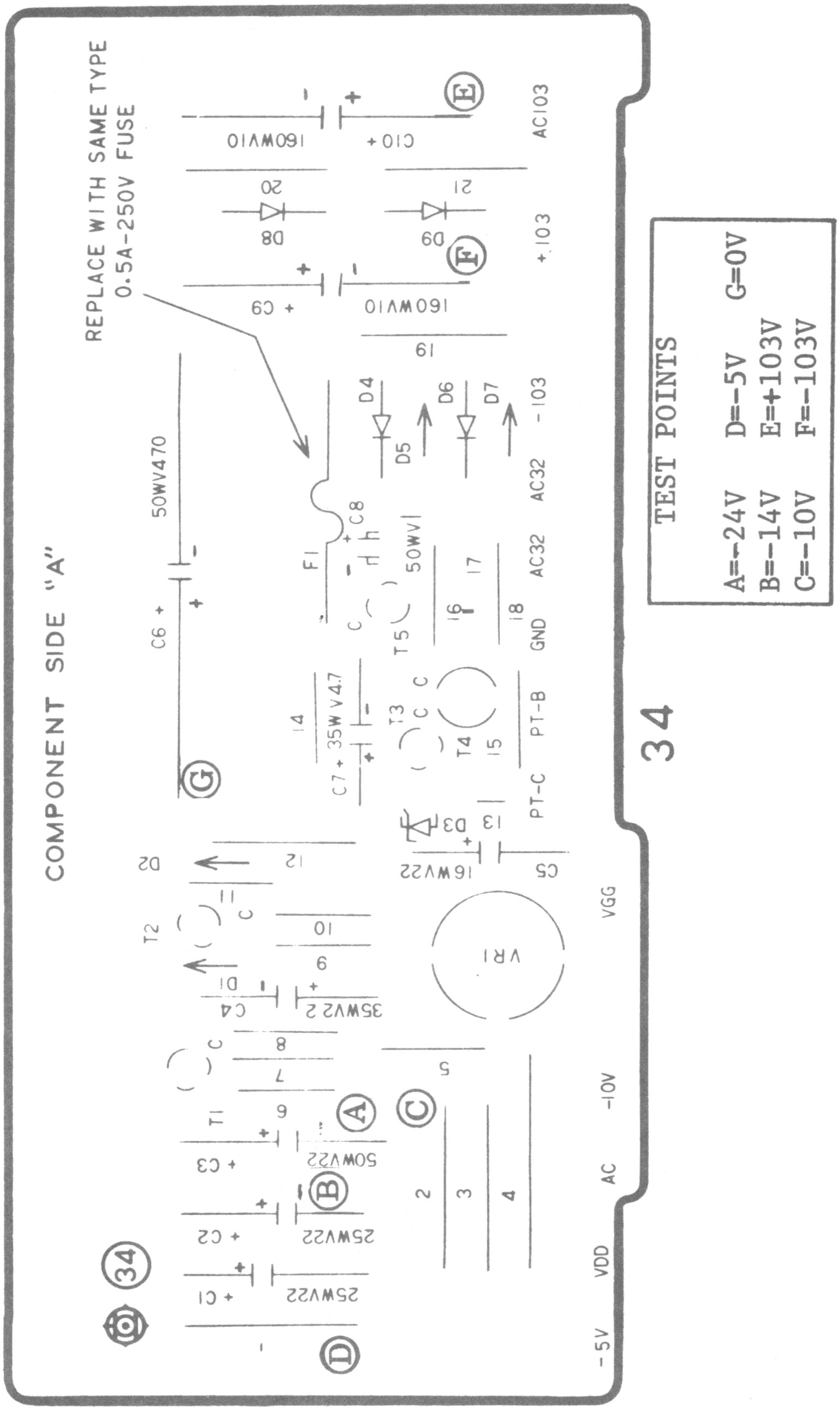


COMPONENT LIST FOR PC CARD #33

P. C. B NO. 33.

MOS IC	22 ① 1/8 100kΩ	56 ① 1/8 470kΩ	90 ① 1/8 100kΩ	124 1/4 2.2MΩ	D DIODE	34 1S84	27 2SA617 Ⓚ	DIODE ARRAY
3-1 HD3103	23 〃 〃 〃	57 〃 〃 〃	91 〃 〃 〃	125 〃 〃	1 1S2075	35 〃	28 〃	91-1 HD9001
2 〃	24 〃 〃 〃	58 〃 〃 100kΩ	92 〃 〃 〃	126 〃 〃	2 〃		29 〃	2 〃
3 〃	25 〃 〃 〃	59 〃 〃 〃	93 〃 〃 27kΩ	127 〃 〃	3 〃		30 〃	3 〃
7-1 HD3107	26 〃 〃 33kΩ	60 〃 〃 〃	94 〃 〃 〃	128 〃 〃	4 〃		31 〃	4 〃
2 〃	27 〃 〃 〃	61 〃 〃 〃	95 〃 〃 100kΩ	129 〃 〃	5 〃		32 〃	5 〃
3 〃	28 〃 〃 〃	62 〃 〃 〃	96 〃 〃 〃		6 〃		33 〃	6 〃
4 〃	29 〃 〃 〃	63 〃 〃 〃	97 〃 〃 〃		7 〃	T TRANSISTOR	34 〃	7 〃
	30 〃 〃 〃	64 〃 〃 〃	98 〃 〃 〃		8 〃	1 2SC284Ⓚ BK	35 〃	8 〃
	31 〃 〃 〃	65 〃 〃 〃	99 〃 〃 27kΩ		9 〃	2 〃	36 2SC284Ⓚ BK	9 〃
	32 〃 〃 〃	66 〃 〃 〃	100 〃 〃 〃		10 〃	3 2SC641Ⓚ	37 2SA617Ⓚ	10 〃
	33 〃 〃 〃	67 〃 〃 56kΩ	101 〃 〃 100kΩ		11 1S84	4 2SC284Ⓚ	38 〃	11 〃
R RESISTOR	34 〃 〃 100kΩ	68 〃 〃 〃	102 〃 〃 〃		12 〃	5 〃	39 〃	12 〃
1 ① 1/8 33kΩ	35 〃 〃 4.7kΩ	69 〃 〃 〃	103 〃 〃 〃		13 〃	6 〃		
2 〃 〃 〃	36 〃 〃 100kΩ	70 〃 〃 〃	104 〃 〃 56kΩ		14 〃	7 〃		
3 〃 〃 〃	37 〃 〃 4.7kΩ	71 〃 〃 〃	105 〃 〃 27kΩ		15 〃	8 〃		
4 〃 〃 〃	38 〃 〃 100kΩ	72 〃 〃 〃	106 〃 〃 4.7kΩ		16 〃	9 〃		
5 〃 〃 27kΩ	39 〃 〃 4.7kΩ	73 〃 〃 〃	107 〃 〃 33kΩ		17 〃	10 〃		
6 〃 〃 33kΩ	40 〃 〃 100kΩ	74 〃 〃 〃	108 〃 〃 22kΩ		18 〃	11 〃	C CAPACITOR	
7 〃 〃 47kΩ	41 〃 〃 4.7kΩ	75 〃 〃 〃	109 〃 〃 100kΩ		19 〃	12 〃	1 200WV 0.15μF	
8 〃 〃 100kΩ	42 〃 〃 100kΩ	76 〃 〃 〃	110 〃 〃 27kΩ		20 〃	13 〃	2 〃 〃	
9 〃 〃 3.3kΩ	43 〃 〃 4.7kΩ	77 〃 〃 4.7kΩ	111 〃 〃 56kΩ		21 1S2075	14 〃	3 〃 〃	
10 〃 〃 22kΩ	44 〃 〃 100kΩ	78 〃 〃 33kΩ	112 〃 〃 22kΩ		22 〃	15 〃	4 〃 〃	
11 〃 〃 〃	45 〃 〃 4.7kΩ	79 〃 〃 〃	113 〃 〃 10kΩ		23 〃	16 〃	5 〃 〃	
12 〃 〃 〃	46 〃 〃 100kΩ	80 〃 〃 22kΩ	114 〃 〃 100kΩ		24 〃	17 〃	6 〃 〃	
13 〃 〃 100kΩ	47 〃 〃 4.7kΩ	81 〃 〃 〃	115 〃 〃 56kΩ		25 〃	18 〃	7 〃 〃	
14 〃 〃 〃	48 〃 〃 100kΩ	82 〃 〃 27kΩ	116 〃 〃 27kΩ		26 〃	19 〃	8 〃 〃	
15 〃 〃 〃	49 〃 〃 4.7kΩ	83 〃 〃 〃	117 〃 〃 〃		27 〃	20 〃	9 〃 〃	
16 〃 〃 〃	50 〃 〃 100kΩ	84 〃 〃 〃	118 1/4 2.2MΩ		28 〃	21 〃	10 〃 〃	
17 〃 〃 〃	51 〃 〃 4.7kΩ	85 〃 〃 100kΩ	119 〃 〃		29 〃	22 〃	11 〃 〃	
18 〃 〃 〃	52 〃 〃 100kΩ	86 〃 〃 〃	120 〃 〃		30 〃	23 〃	12 〃 〃	
19 〃 〃 〃	53 〃 〃 4.7kΩ	87 〃 〃 〃	121 〃 〃		31 〃	24 〃		
20 〃 〃 〃	54 〃 〃 100kΩ	88 〃 〃 〃	122 〃 〃		32 〃	25 〃		
21 〃 〃 〃	55 〃 〃 〃	89 〃 〃 27kΩ	123 〃 〃		33 〃	26 2SA617Ⓚ		

LOGIC CARD #34 (Power Supply)

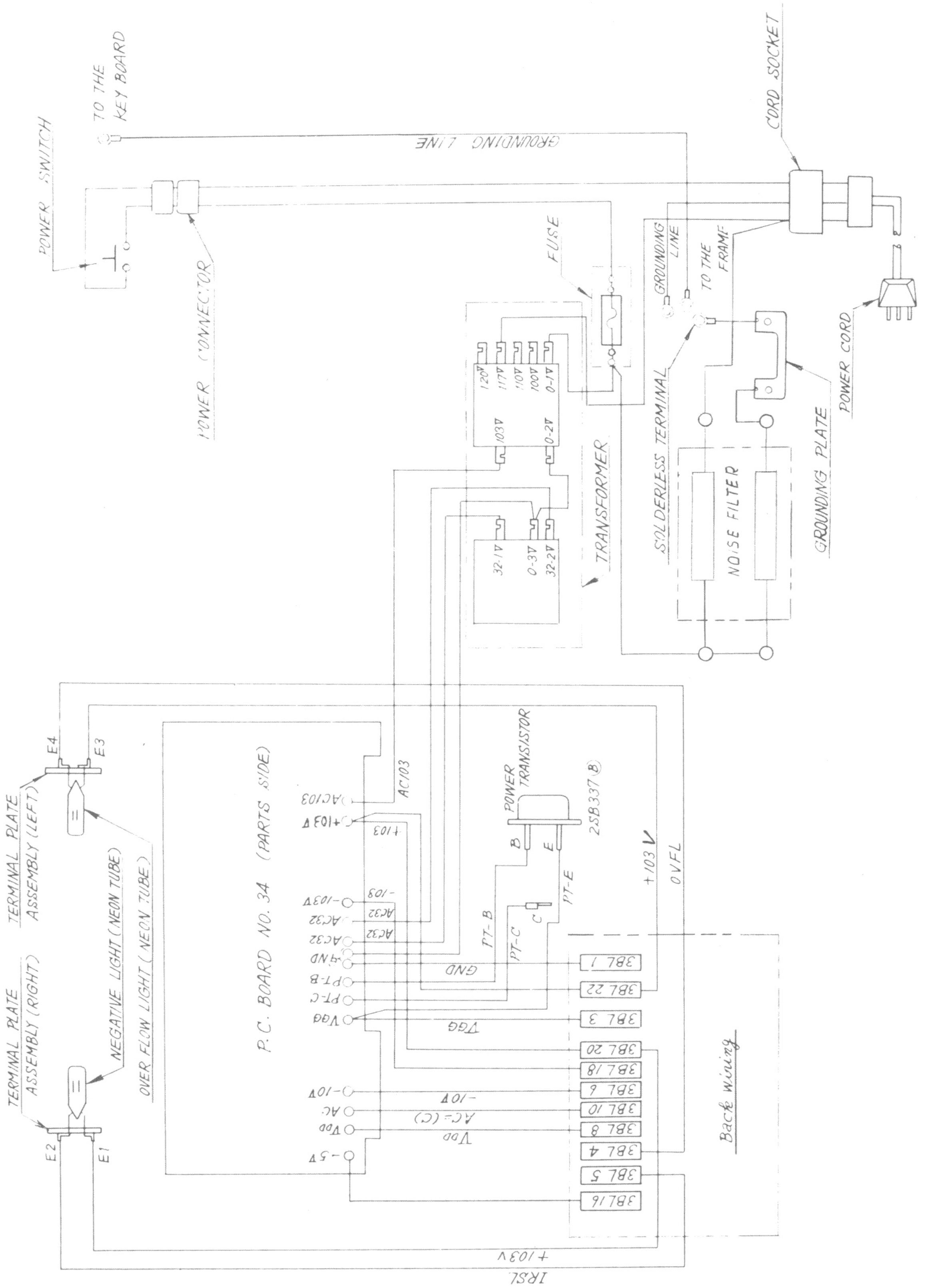


COMPONENT LIST FOR PC CARD #34

P. C. B NO. 34

R	RESISTOR	D	DIODE	T	TRANSISTOR
1	1W 68Ω	1	1S2075	1	2SA617 Ⓚ
2	〃 220Ω	2	〃	2	2SB77 Ⓐ
3	〃 100Ω	3	1S760Ⓗ	3	〃
4	2W100Ω	4	V06C	4	2SB89
5	1/8 1.5kΩ	5	1S84	5	2SB77 Ⓐ
6	〃 8.2kΩ	6	V06C		
7	〃 22kΩ	7	1S84		
8	〃 8.2kΩ	8	V06C		
9	〃 22kΩ	9	〃		
10	〃 15kΩ				VARIABLE RESISTOR
11	〃 2.2kΩ			VR1	1/10 1kΩB
12	1/4 3.3kΩ				
13	Ⓤ 1/4 2.2kΩ				
14	1/8 10kΩ				
15	〃 〃				
16	〃 18kΩ	C	CAPACITOR		
17	Ⓤ 1/8 10kΩ	1	25WV 22μF	F	FUSE
18	1/8 18kΩ	2	〃 〃	1	0.5A 250V
19	1/4 100kΩ	3	50WV 〃		
20	〃 〃	4	35WV 4.7μF		
21	〃 470Ω	5	16WV 22μF		
		6	50WV 470μF		
		7	35WV 4.7μF		
		8	50WV 1μF		
		9	16WV 10μF		
		10	〃 〃		

I. POWER SUPPLY WIRING DIAGRAM



J. WIRING LISTS & SIGNAL NAME CROSS REFERENCE

SIGNAL OF TERMINAL (IN P.C. BOARD CONNECTOR)

P.C.B. Face	Pin No.	31 A	31 B	32 A	32 B	33 A	33 B	Pin No.	P.C.B. Face
L	1	$\overline{WT2CP1}$	GND	8	GND	1	GND	1	L
	2	D	R2P=12	4		$\overline{2}$	OVF2	2	
	3	M	VGG	$\overline{8}$	VGG	8	VGG	3	
	4	MDF	VDD	XC2		$\overline{8}$	OVFL	4	
	5	S_{OVF2}	AOS	FAS SUB	VDD	4	IRSL	5	
	6	FAS SUB	X0	1	BT4	$\overline{1}$	−10V	6	
	7	XC4	OSF	2	FA	$\overline{4}$	(DT1)	7	
	8	R2No>4	RSH	$\overline{4}$	$\overline{1}$	2	VDD	8	
	9	MLT2+DIV2	DIV2	R/0F·KR/0	XC3		DT1	9	
	10	FA	K7	XC4	R2No>4	S_{IRS}		10	
	11	BT2	XC3	R3	FCIN	DT2		11	
	12	CDP	N1	(X0)	C+AC	DT3		12	
	13	K3	CWF	$\overline{DT1+DT2}$	$\overline{2}$	DT4		13	
	14	N	BD		DT1	$\overline{BT4CP1}$		14	
	15	DT2	DT2·BT1	DIV2	R2			15	
	16	BT1	WT1	N+P	K·(MLT2+DIV2)(MLT1+DIV1)	$\overline{CP2}$	−5V	16	
	17	K6	N2	CHG	(R3)			17	
	18	R2	C+AC+CE	$\overline{ENT}$	CDP		−103V	18	
	19	S_{IRS}	BT3	BD	LSH+RSH			19	
	20	R3	K5	MDF	AOS		+103V	20	
	21	DT1	DT16	LSH	CWF			21	
	22	LSH+RSH	N3	R/0F	DT4	DT16		22	
R	1	BT4	K9	$\overline{BT4CP1}$	WT1			1	R
	2	$\overline{BT4CP1}$	C+AC	RSH	S_{OSF}			2	
	3	N4	FP2	KFF2	S			3	
	4	LSH	R/0F	(BT1)	X0			4	
	5	FP5	DT1+DT2	DT2·BT4	OVF1			5	
	6	S_{OSF}	R	R1	TC=16			6	
	7	A	CP1	S_{OVF2}	OP			7	
	8	S	CHG	R2P=12	N			8	
	9	OVF1	KEY COMMON	BT1	POT			9	
	10	P	XC2	C+AC+CE	OVF2			10	
	11	N+P	CP2		OSF			11	
	12	DT3	KFF2	$\overline{CP2}$	(R2)			12	
	13	R/0F·KR/0	OVF2	DT1+DT2	DT2·BT1			13	
	14	TC=16	KF COMMON	$\overline{CP1}$	DT3			14	
	15	$\overline{DT1+DT2}$	K·(MLT2+DIV2)	DT2	BT2			15	
	16	(WT2)	$\overline{CP1}$	$\overline{WT2CP1}$	BT3			16	
	17	DT4	WT2	DT16	$\overline{WTCP1}$			17	
	18	R1	$\overline{ENT}$	$\overline{(CP1M)}$	MLT2+DIV2			18	
	19	DT2·BT4	FP COMMON		CP1			19	
	20	FCIN	K·(MLT2+DIV2)(MLT1+DIV1)		$\overline{(CP2M)}$			20	
	21	OP	$\overline{WTCP1}$		$\overline{CP1M}$			21	
	22	POT	(KFF2)	WT2	$\overline{CP2M}$			22	

BACK WIRING

BACK WIRING

SIGNAL	TERMINAL NUMBER			
$\overline{CP1}$	1BR16	2AR14		
$\overline{CP2}$	1BR11	2AR12	3AL16	
CP1	1BR7	2BR19		
$\overline{CP1M}$	2BR21			D-36
$\overline{CP2M}$	2BR22			D-38
($\overline{CP1M}$)	2AR18			D-37
($\overline{CP2M}$)	2BR20			D-39
$\overline{WTCP1}$	1BR21	2BR17		
$\overline{WT2CP1}$	1AL1	2AR16		
BT4CP1	1AR2	2AR1	3AL14	
WT1	1BL16	2BR1		
WT2	1BR17	2AR22		D-40
(WT2)	1AR16			D-41
DT1	1AL21	2BL14	3BL9	D-30
$\overline{DT2}$	1AL15	2AR15	3AL11	
$\overline{DT3}$	1AR12	2BR14	3AL12	
DT4	1AR17	2BL22	3AL13	
DT16	1BL21	2AR17	3AL22	
(DT1)	3BL7			D-31
$\overline{DT_1+DT_2}$	1BR5	2AR13		
$\overline{DT_1}+DT_2$	1AR15	2AL13		
$DT_2 \cdot BT_1$	1BL15	2BR13		
$DT_2 \cdot BT_4$	1AR19	2AR5		
BT1	1AL16	2AR9		D-42
BT2	1AL11	2BR15		
BT3	1BL19	2BR16		
BT4	1AR1	2BL6		
(BT1)	2AR4			D-43
FP COMMON	1BR19			D-28
FP2	1BR3			D-12
FP5	1AR5			D-13
R1	1AR18	-2AR6		
R2	1AL18	2BL15	2BR12	D-32
R3	1AL20	2AL11	2BL17	
OP	1AR21	2BR7		
X0	1BL6	2AL12	2BR4	
XC2	1BR10	2AL4		
XC3	1BL11	2BL9		
XC4	1AL7	2AL10		

SIGNAL	TERMINAL NUMBER			
FAS SUB	1AL6	2AL5		
FA	1AL10	2BL7		
FCIN	1AR20	2BL11		
R2N0>4	1AL8	2BL10		
R2P=12	1BL2	2AR8		
TC=16	1AR14	2BR6		
MDF	1AL4	2AL20		
SOVF2	1AL5	2AR7		
OVF1	1AR9	2BR5		
OVF2	1BR13	2BR10	3BL2	D-33
SIRS	1AL19	3AL10		
SOSF	1AR6	2BR2		
CWF	1BL13	2BL21		
RSH	1BL8	2AR2		
LSH	1AR4	2AL21		
CHG	1BR8	2AL17		
$\overline{LSH+RSH}$	1AL22	2BL19		
AOS	1BL5	2BL20		
OSF	1BL7	2BR11		
POT	1AR22	2BR9		
$\overline{CDP}$	1AL12	2BL18		
$\overline{ENT}$	1BR18	2AL18		
DIV2	1BL9	2AL15		
MLT2+DIV2	1AL9	2BR18		D-29
$K\cdot(MLT_2+DIV_2)(\overline{MLT_1+DIV_1})$	1BR20	2BL16		
R/0 F	1BR4	2AL22		D-11
R/0 F·K R/0	1AR13	2AL9		D-25
KFF2	1BR12	2AR3		D-44
(KFF2)	1BR22			D-45
KF COMMON	1BR14			D-15
KEY COMMON	1BR9			D-19
N+P	1AR11	2AL16		
N	1AL14	2BR8		D-6
P	1AR10			D-23
N1	1BL12			D-1
N2	1BL17			D-20
N3	1BL22			D-5
N4	1AR3			D-26
$K\cdot(MLT_2+DIV_2)$	1BR15			D-16

SIGNAL	TERMINAL NUMBER			
BD	1BL14	2AL19		
K3	1AL13			D-4
K5	1BL20			D-27
K6	1AL17			D-9
K7	1BL10			D-10
K9	1BR1			D-14
A	1AR7			D-8
S	1AR8	2BR3		D-21
M	1AL3			D-24
D	1AL2			D-2
R	1BR6			D-22
C+AC	1BR2	2BL12		D-3-4
C+AC+CE	1BL18	2AR10		D-7
1	2AL6	3AL1		
$\overline{1}$	2BL8	3AL6		
2	2AL7	3AL8		
$\overline{2}$	2BL13	3AL2		
4	2AL2	3AL5		
$\overline{4}$	2AL8	3AL7		
8	2AL1	3AL3		
$\overline{8}$	2AL3	3AL4		
VGG	1BL3	2BL3	3BL3	
VDD	1BL4	2BL5	3BL8	
GND	1BL1	2BL1	3BL1	D-17
-5V	3BL16			
-10V	3BL6			
+103V	3BL20			
-103V	3BL18			
OVFL	3BL4			
IRSL	3BL5			

INTERCONNECTION BETWEEN REMOVABLE SUB CONNECTOR AND KEYBOARD

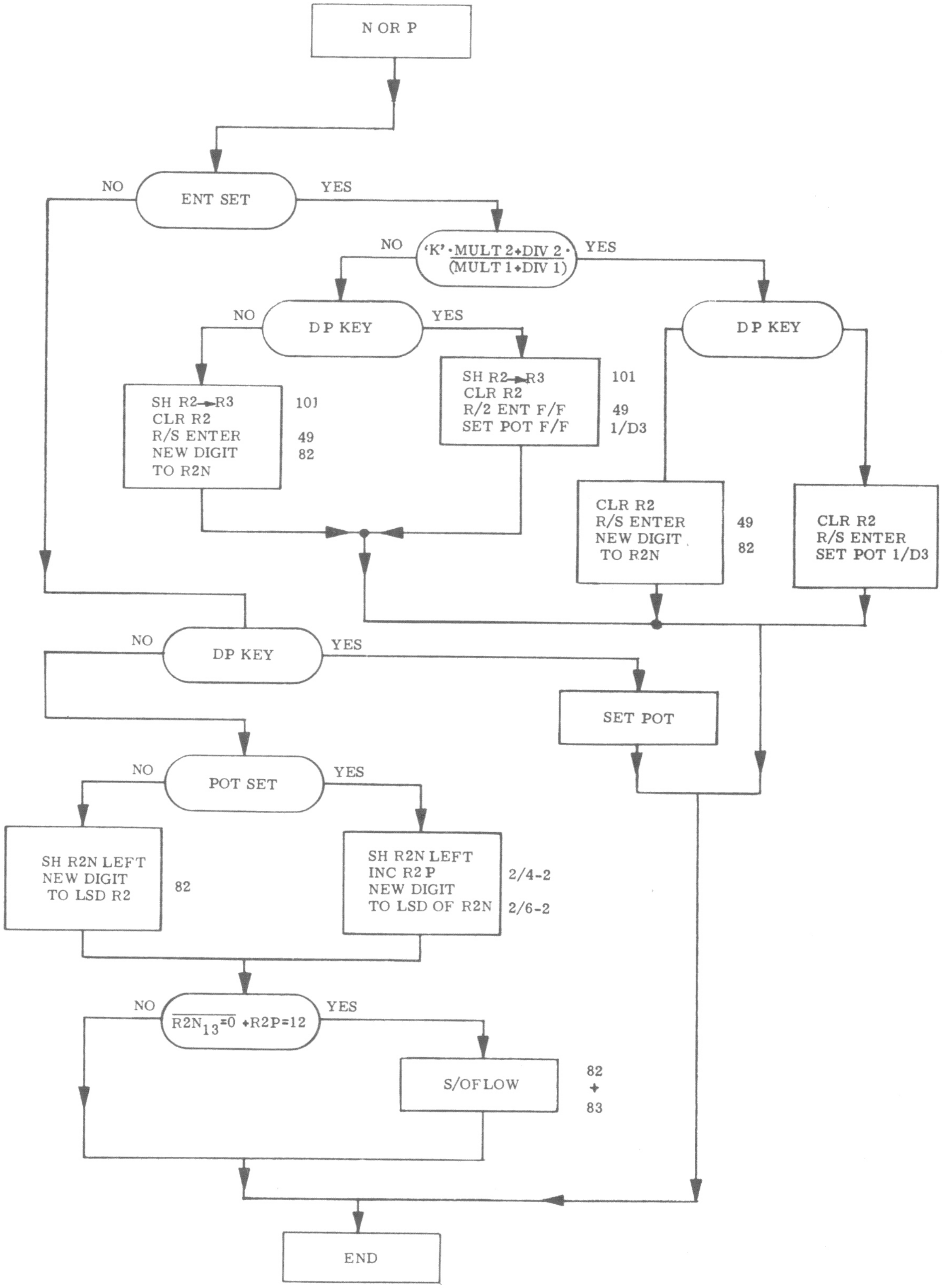
SIGNAL	TERMINAL NUMBER	
	SUB CONNECTOR	KEY BOARD
N1	C1	A 28
D	C2	A 4
C+AC	C3	A 32
K3	C4	A 23
N3	C5	A 25
N	C6	A 27
C+AC+CE	C7	A 29
A	C8	A 13
K6	C9	A 17
K7	C10	A 20
R/0F	C11	A 14
FP2	C12	B 2
FP5	C13	B 4
K9	C14	A 16
KF COMMON	C15	A 3
K·(MLT2+DIV2)	C16	A 34
GND	C17	A 30
KEY COMMON	C19	A 24
N2	C20	A 26
S	C21	A 10
R	C22	A 11
P	C23	A 22
M	C24	A 12
R/0 F·K R/0	C25	A 15
N4	C26	A 21
K5	C27	A 19
FP COMMON	C28	B 3
MLT2+DIV2	C29	A 33
DT1	C30 (C31)	
R2	C32	
OVF2	C33	
$\overline{CP1M}$	C36 (C37)	
$\overline{CP2M}$	C38 (C39)	
WT2	C40 (C41)	
BT1	C42 (C43)	
KFF2	C44 (C45)	

SECTION 6

FLOW CHARTS

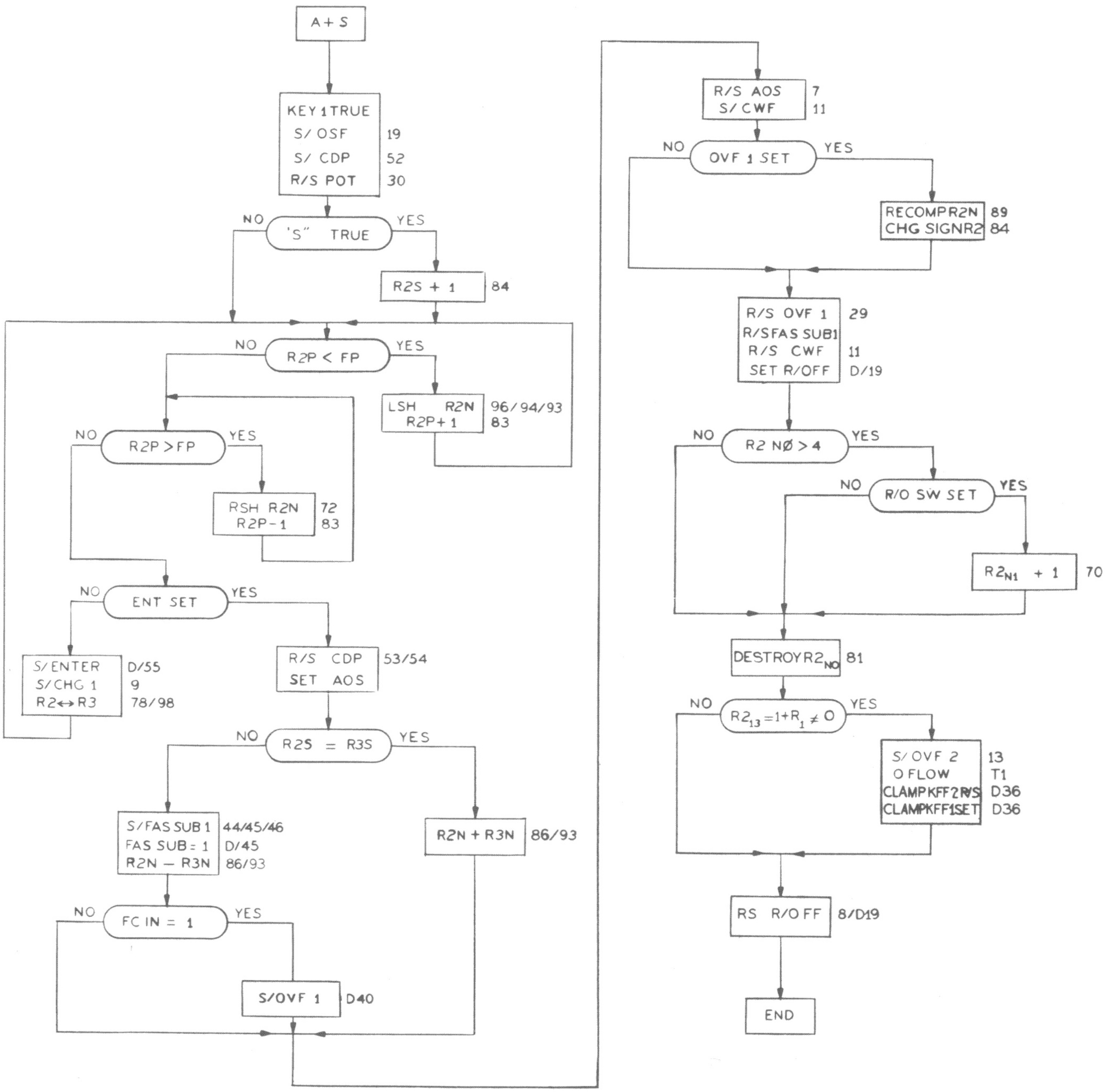
SECTION CONTENTS

A. ENTRY

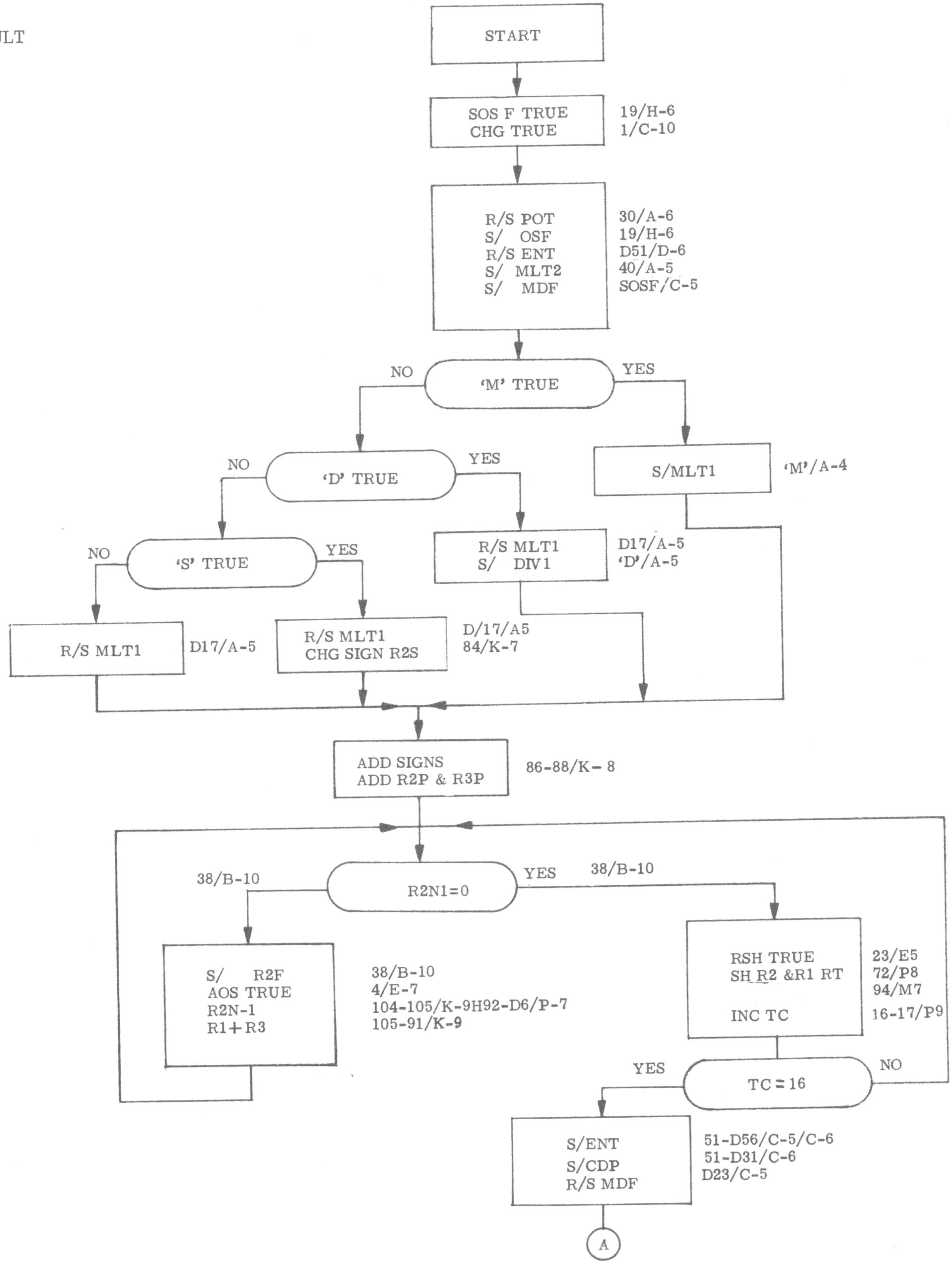


EC 1115

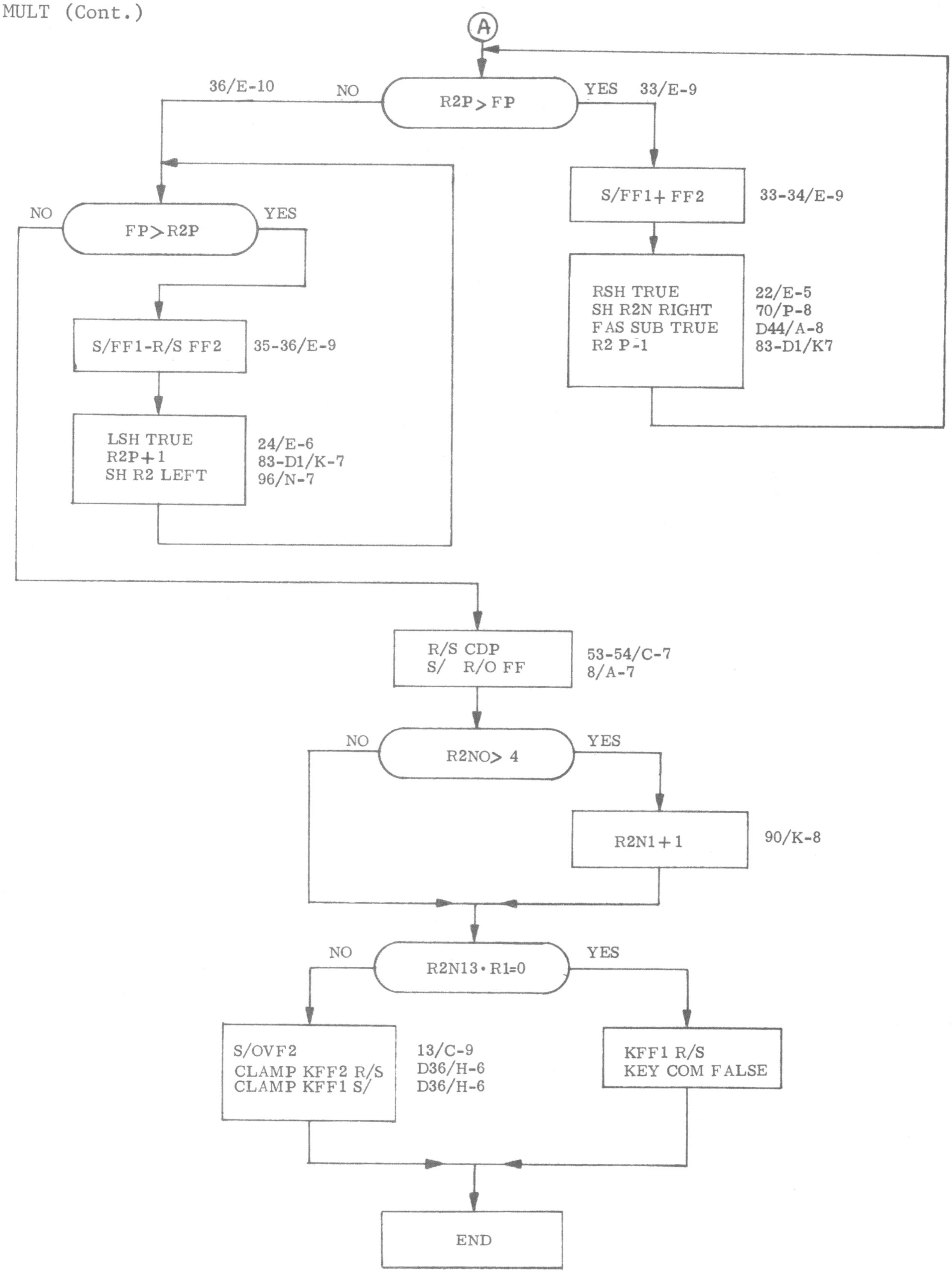
B. ADD OR SUBTRACT



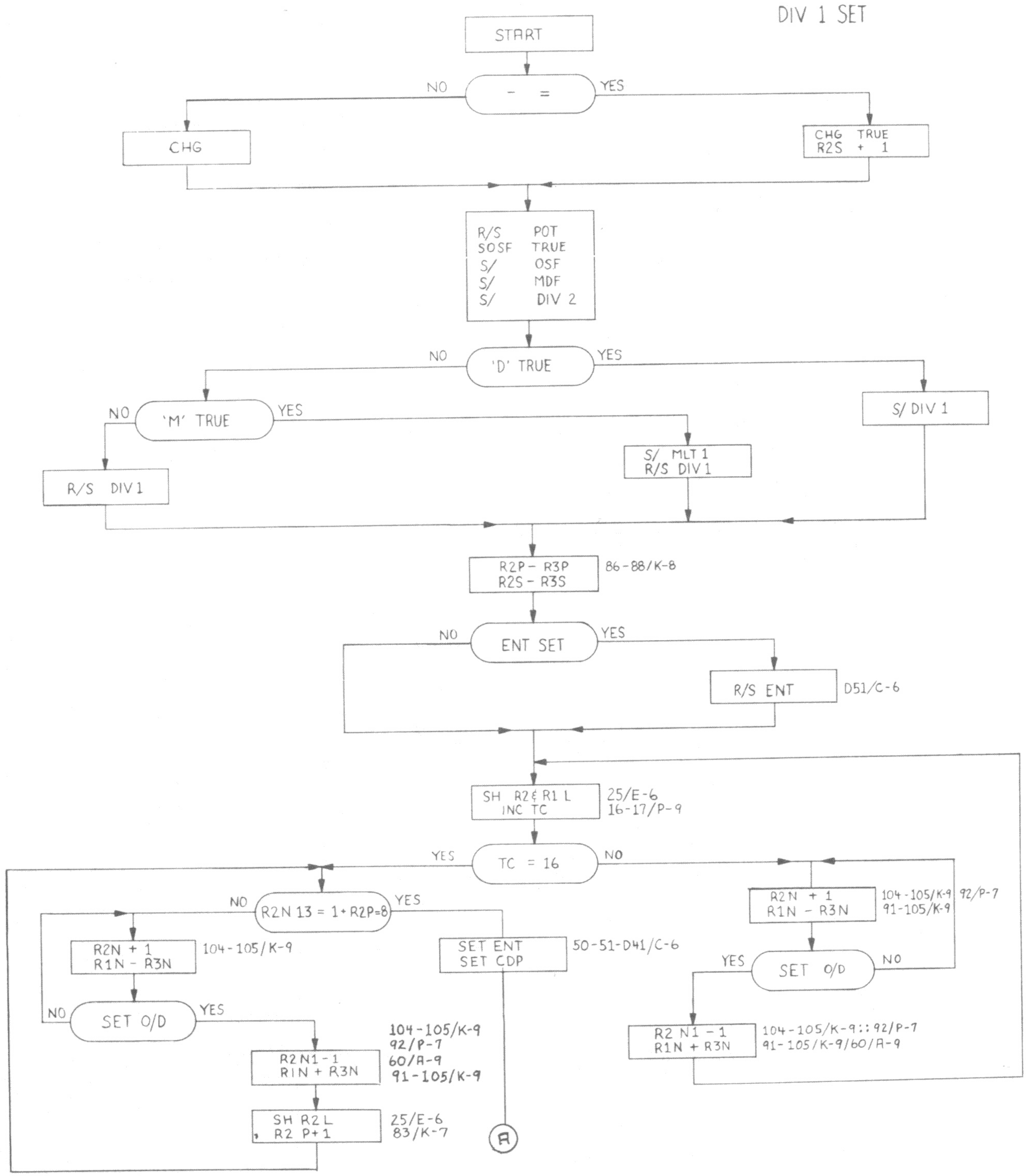
C. MULT


START
SOS F TRUE
CHG TRUE
19/H-6
1/C-10
R/S POT
S/ OSF
R/S ENT
S/ MLT2
S/ MDF
30/A-6
19/H-6
D51/D-6
40/A-5
SOSF/C-5
NO
'M' TRUE
YES
S/MLT1
'M'/A-4
NO
'D' TRUE
YES
R/S MLT1
S/ DIV1
D17/A-5
'D'/A-5
NO
'S' TRUE
YES
R/S MLT1
D17/A-5
R/S MLT1
CHG SIGN R2S
D/17/A5
84/K-7
ADD SIGNS
ADD R2P & R3P
86-88/K- 8
38/B-10
R2N1=0
YES
38/B-10
S/ R2F
AOS TRUE
R2N-1
R1+R3
38/B-10
4/E-7
104-105/K-9H92-D6/P-7
105-91/K-9
RSH TRUE
SH R2 &R1 RT
INC TC
23/E5
72/P8
94/M7
16-17/P9
YES
TC=16
NO
S/ENT
S/CDP
R/S MDF
51-D56/C-5/C-6
51-D31/C-6
D23/C-5
A

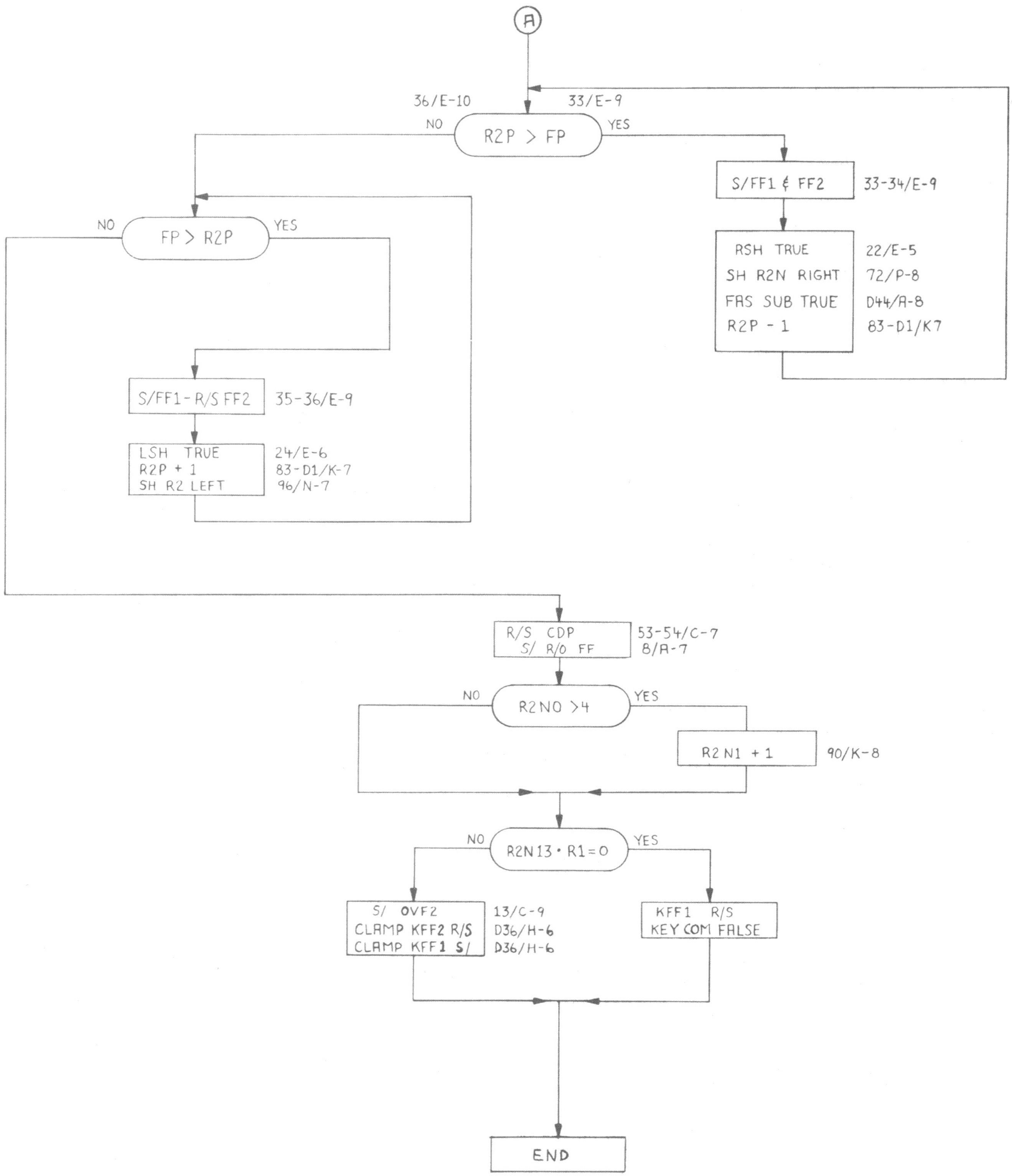
C. MULT (Cont.)


A
36/E-10
NO
R2P > FP
YES
33/E-9
S/FF1+ FF2
33-34/E-9
RSH TRUE
SH R2N RIGHT
FAS SUB TRUE
R2 P -1
22/E-5
70/P-8
D44/A-8
83-D1/K7
NO
FP > R2P
YES
S/FF1-R/S FF2
35-36/E-9
LSH TRUE
R2P+1
SH R2 LEFT
24/E-6
83-D1/K-7
96/N-7
R/S CDP
S/ R/O FF
53-54/C-7
8/A-7
NO
R2NO> 4
YES
R2N1+1
90/K-8
NO
R2N13 • R1=0
YES
S/OVF2
CLAMP KFF2 R/S
CLAMP KFF1 S/
13/C-9
D36/H-6
D36/H-6
KFF1 R/S
KEY COM FALSE
END

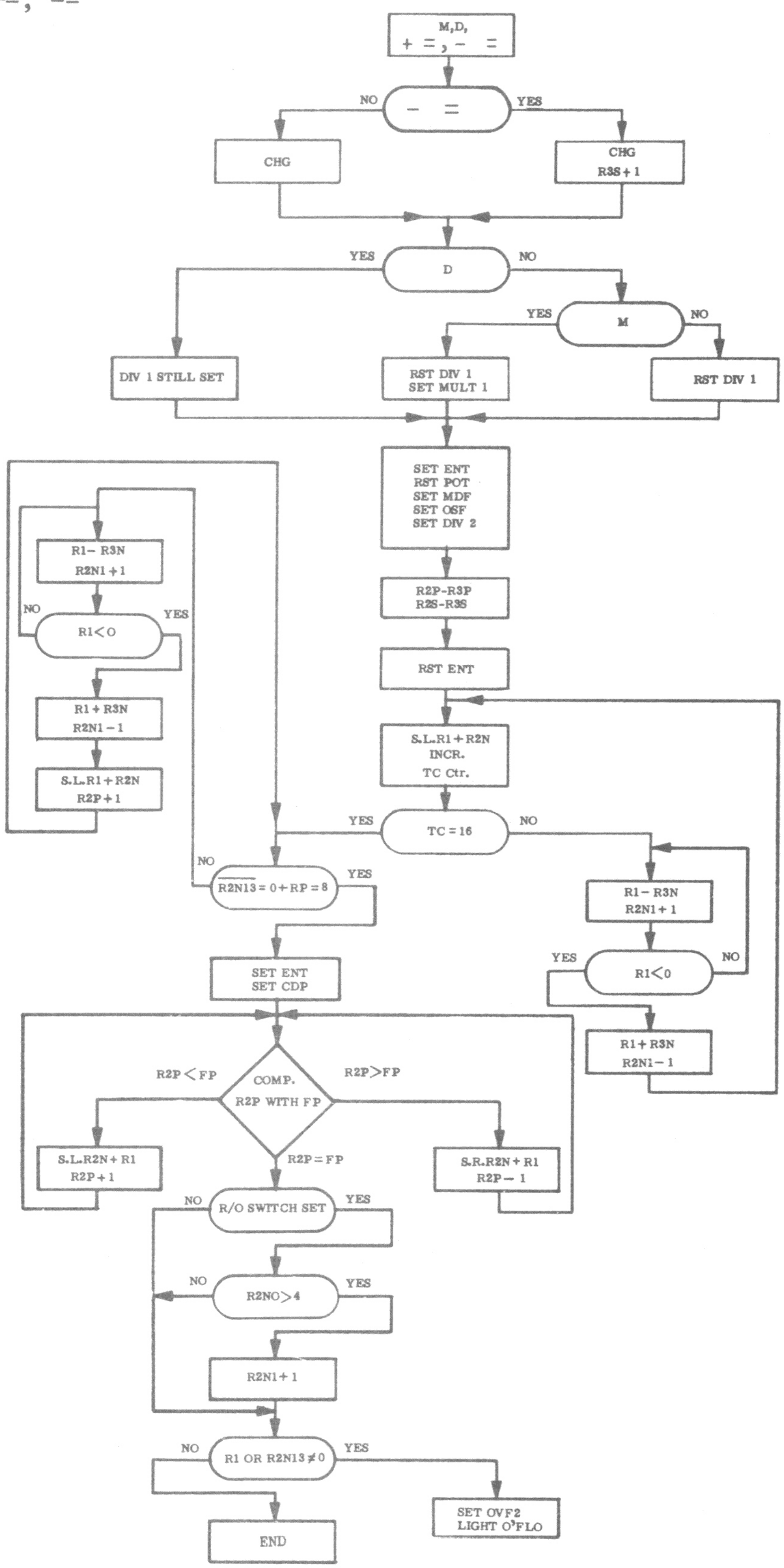
D. DIVIDE


DIV 1 SET
START
NO
− =
YES
CHG
CHG TRUE
R2S + 1
R/S POT
SOSF TRUE
S/ OSF
S/ MDF
S/ DIV 2
NO
'D' TRUE
YES
NO
'M' TRUE
YES
S/ DIV 1
S/ MLT 1
R/S DIV 1
R/S DIV 1
R2P − R3P
R2S − R3S
86-88/K-8
NO
ENT SET
YES
R/S ENT
D51/C-6
SH R2 & R1 L
INC TC
25/E-6
16-17/P-9
YES
TC = 16
NO
NO
R2N 13 = 1 + R2P=8
YES
R2N + 1
R1N − R3N
104-105/K-9 92/P-7
91-105/K-9
R2N + 1
R1N − R3N
104-105/K-9
SET ENT
SET CDP
50-51-D41/C-6
YES
SET O/D
NO
NO
SET O/D
YES
R2 N1 − 1
R1N + R3N
104-105/K-9 :: 92/P-7
91-105/K-9/60/A-9
104-105/K-9
92/P-7
60/A-9
91-105/K-9
R2 N1 − 1
R1N + R3N
SH R2 L
R2 P+1
25/E-6
83/K-7
A

D. DIVIDE (Cont.)



E. M, D, +=, -=


M,D,
+ =, - =
- =
NO
YES
CHG
CHG
R3S + 1
D
YES
NO
M
YES
NO
DIV 1 STILL SET
RST DIV 1
SET MULT 1
RST DIV 1
SET ENT
RST POT
SET MDF
SET OSF
SET DIV 2
R2P-R3P
R2S-R3S
RST ENT
S.L.R1 + R2N
INCR.
TC Ctr.
TC = 16
YES
NO
R1 - R3N
R2N1 + 1
R1<0
YES
NO
R1 + R3N
R2N1 - 1
R1 - R3N
R2N1 + 1
R1<O
NO
YES
R1 + R3N
R2N1 - 1
S.L.R1 + R2N
R2P + 1
R2N13 = 0 + RP = 8
NO
YES
SET ENT
SET CDP
COMP.
R2P WITH FP
R2P<FP
R2P>FP
R2P = FP
S.L.R2N + R1
R2P + 1
S.R.R2N + R1
R2P - 1
R/O SWITCH SET
NO
YES
R2NO>4
NO
YES
R2N1 + 1
R1 OR R2N13 ≠ 0
NO
YES
END
SET OVF2
LIGHT O'FLO